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ISSCC 2014
SESSION 22
High-Speed Data Converters

A 90GS/s 8b 667mW 64x Interleaved SAR ADC in 32nm Digital SOI CMOS

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Outline

- Motivation
- Applications
- ADC overview
- Interleaver
- Sub-ADC
- Experimental results
- Summary

Motivation

- Build an ADC in CMOS for ITU-OTU4 (100Gb/s)
- How far can one go in speed, power and area in 32nm SOI CMOS?
- Find and implement a promising architecture for the interleaver

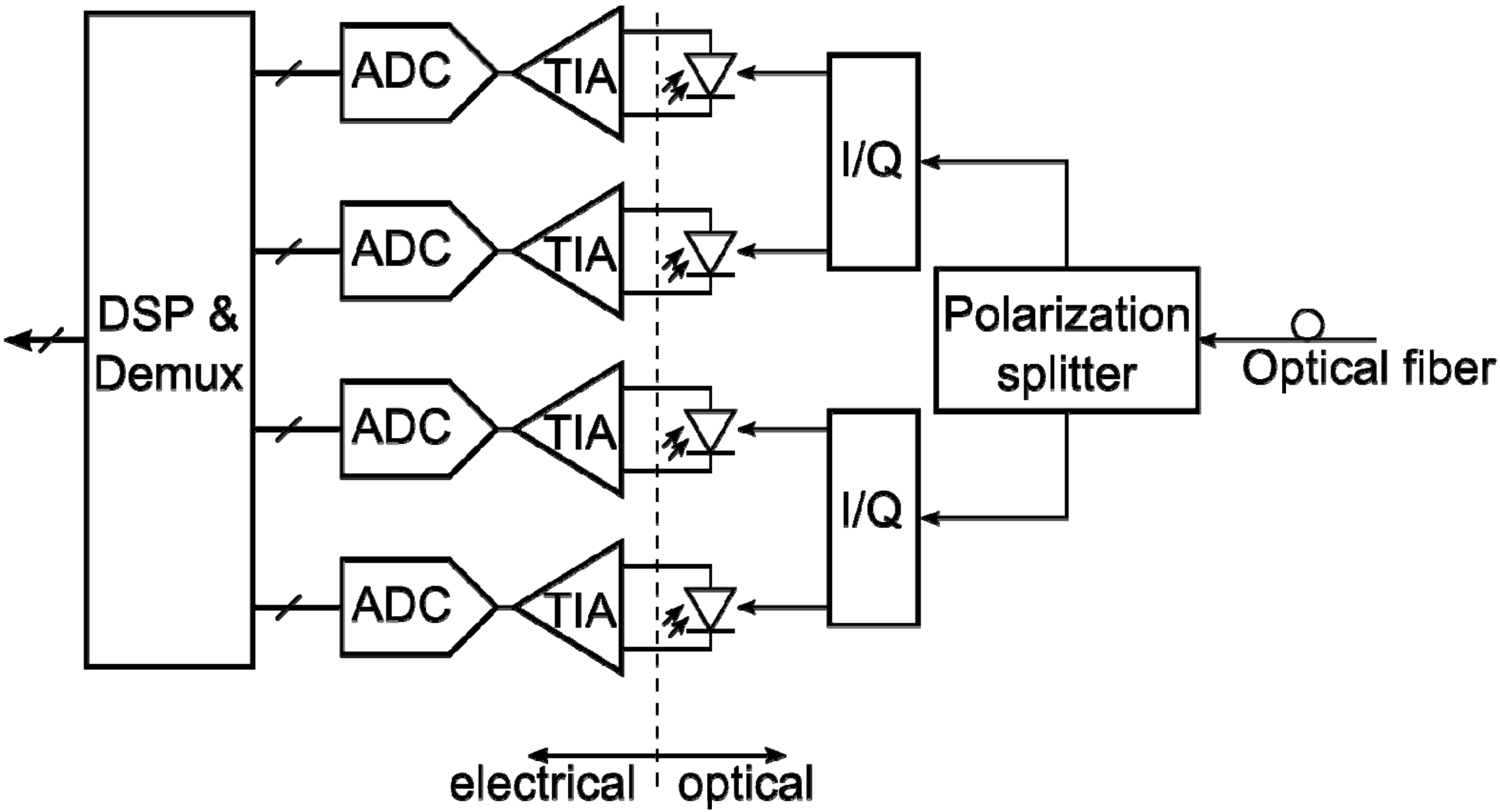
Target ADC Specs

- 55-65 GS/s
- 8 bits
- 6 ENOB at DC, 5.5 ENOB at 16G
- > 16GHz bandwidth
- Lowest power and area

ITU-OTU4

- Used for long-range Internet backbone
- Optical standard at 100Gb/s
- One wavelength, 2 polarizations
- I/Q modulation
- 4 signal paths, 25Gb/s each
  → requires 4 ADCs per 100Gb/s

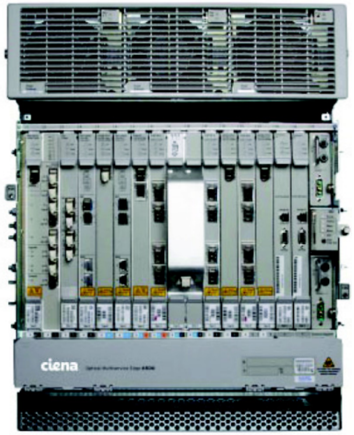
ITU-OTU4



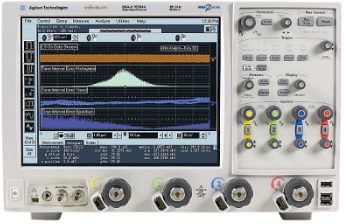
DSP &
Demux
ADC
TIA
ADC
TIA
ADC
TIA
ADC
TIA
I/Q
I/Q
Polarization
splitter
Optical fiber
electrical
optical

Other applications

- Data Communication Networks
  - 100 Gb/s Ethernet (802.3bj)
  - 400 Gb/s ITU-OTU5 and Metro
  - Fiber to the home
  - Passive optical networks
- Measurement equipment
  - Oscilloscopes
- Radar
  - Potentially higher resolution required

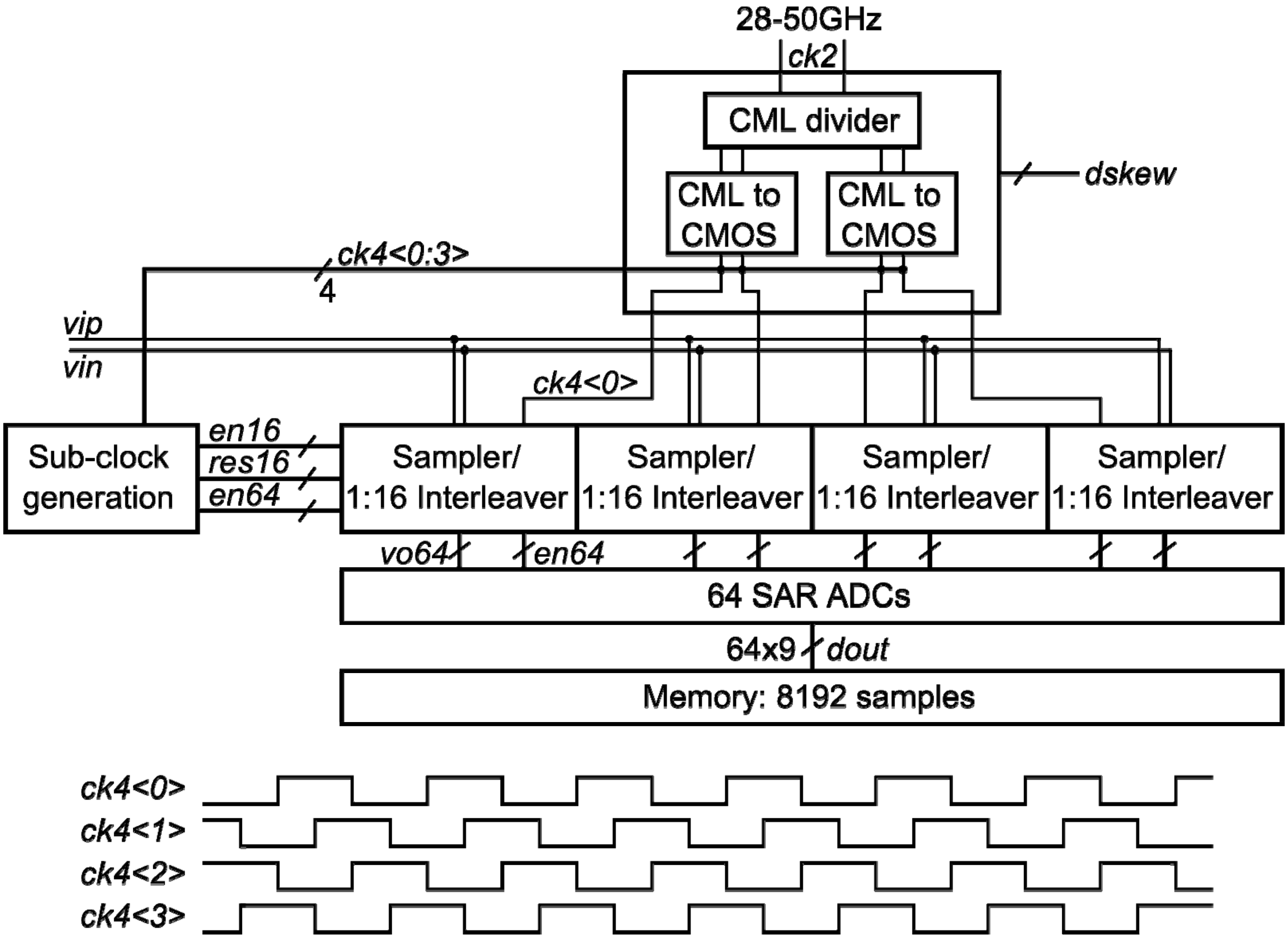


[ciena.com]



[agilent.com]

ADC overview

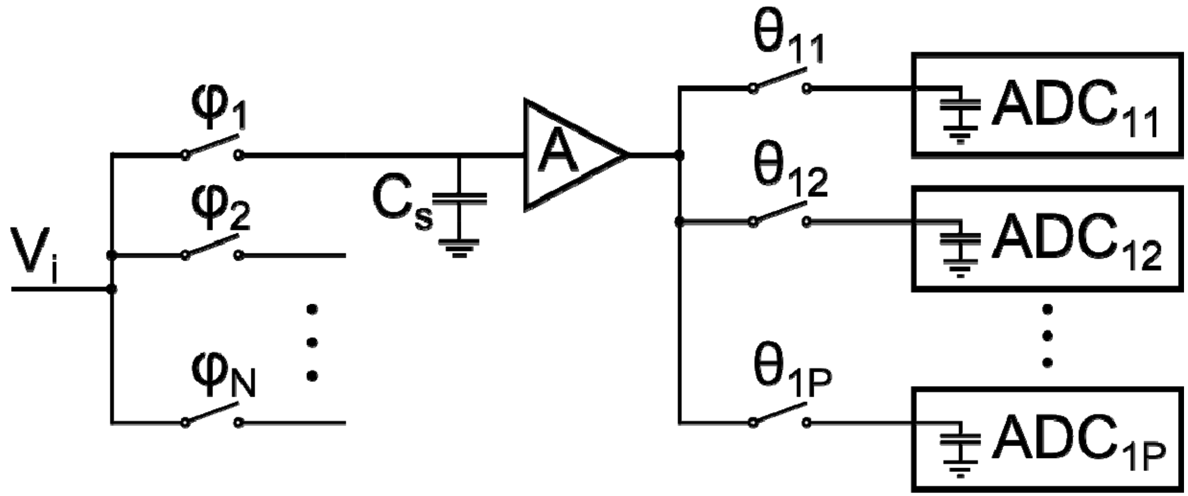


Interleaver

- Solution has to provide:
  - High bandwidth
  - Small number of critical clock phases
  - Long enough hold time
  - High linearity
- Technology:
  - IBM 32nm SOI CMOS*

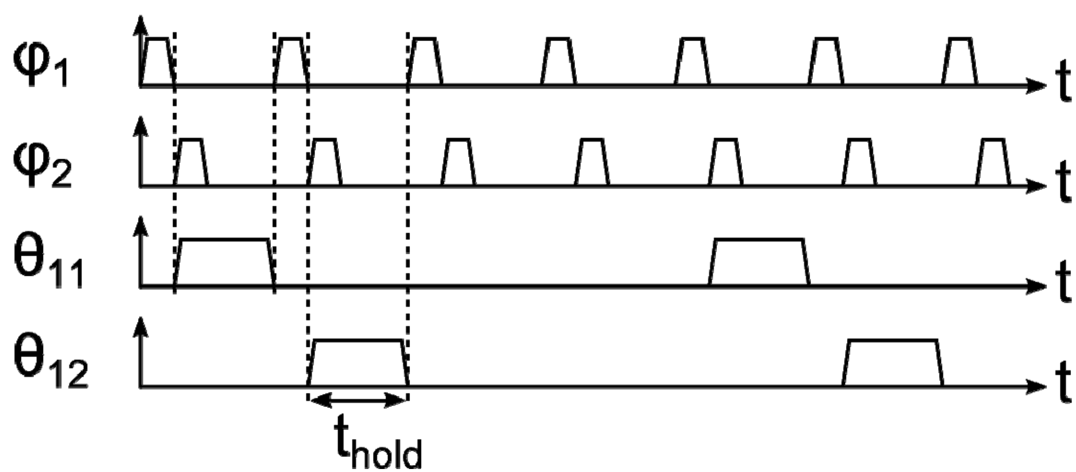
*S. Lee, et al., “Advanced modeling and optimization of high performance 32nm HKMG SOI CMOS for RF/analog SoC applications”, VLSI Symposium, 2012

Sub-sampling



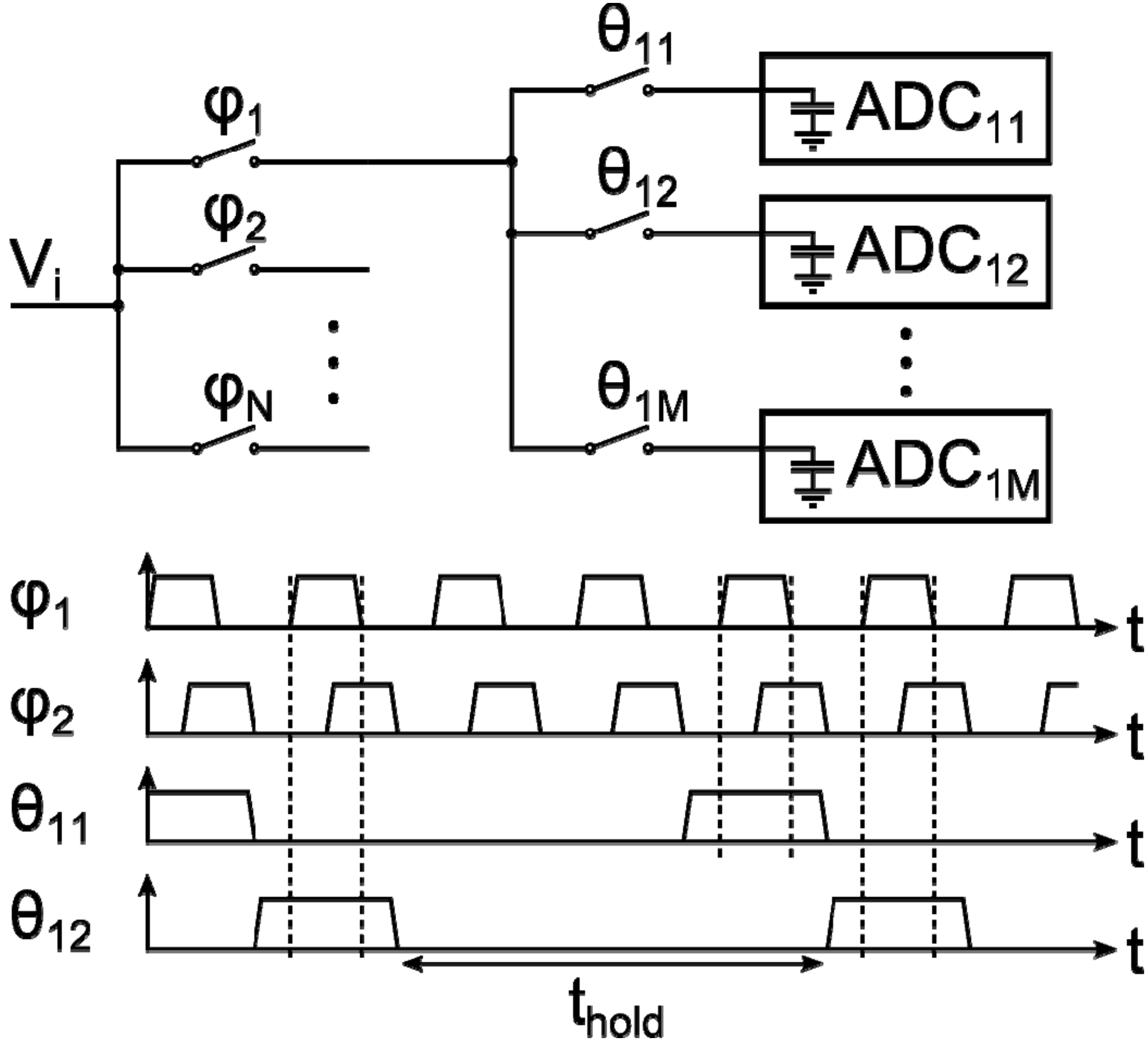
Hold time on C_s for N channels:

N	t_{hold}
4	3 T_s
8	7 T_s



$T_s = 1/f_s = 11ps@90GHz$

Sampling with inline demux



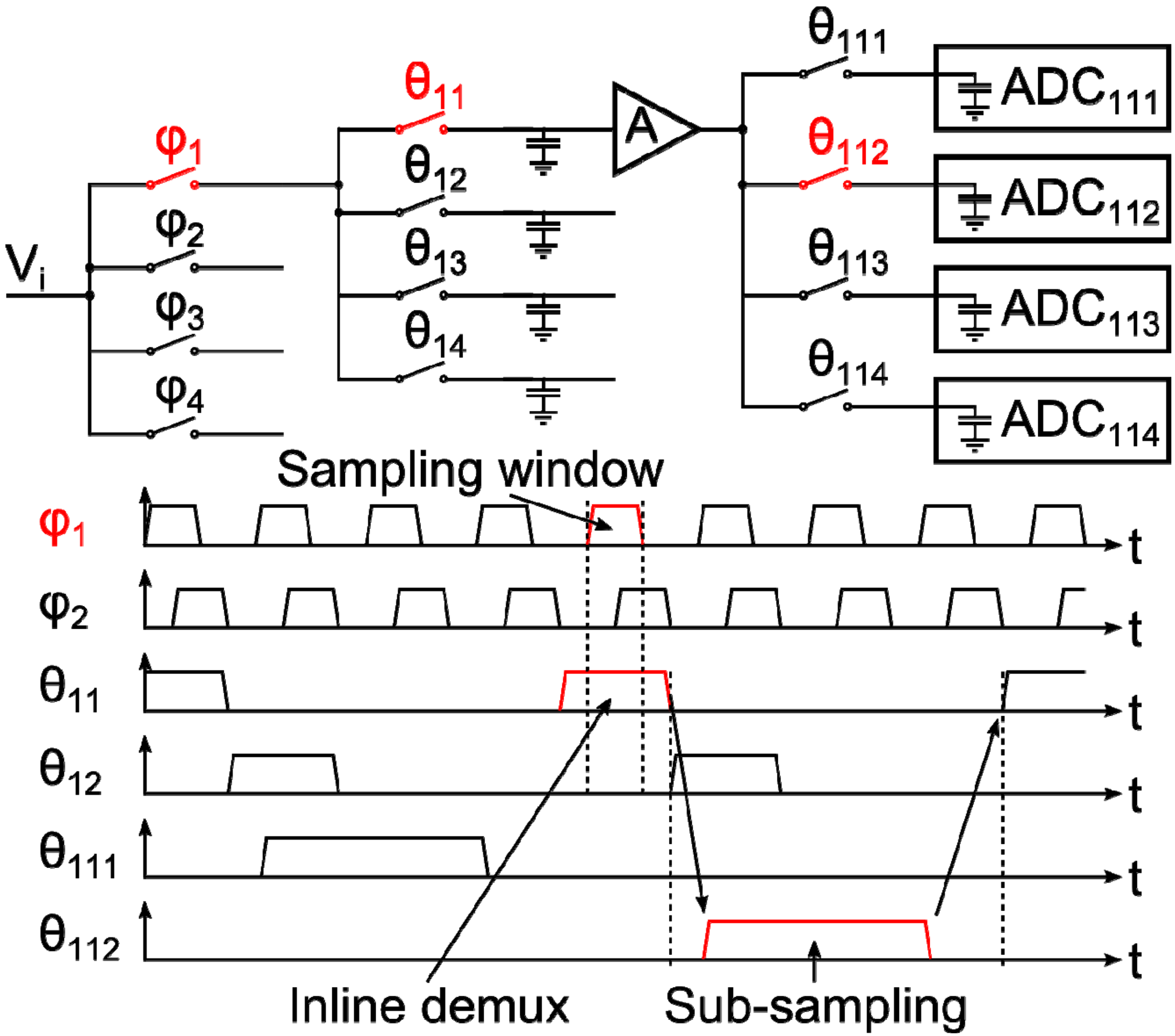
Hold time on ADC
for N x M channels:

N	M	t_{hold}
1	4	3 T_s
2	4	6 T_s
4	2	4 T_s
4	4	12 T_s
4	8	28 T_s

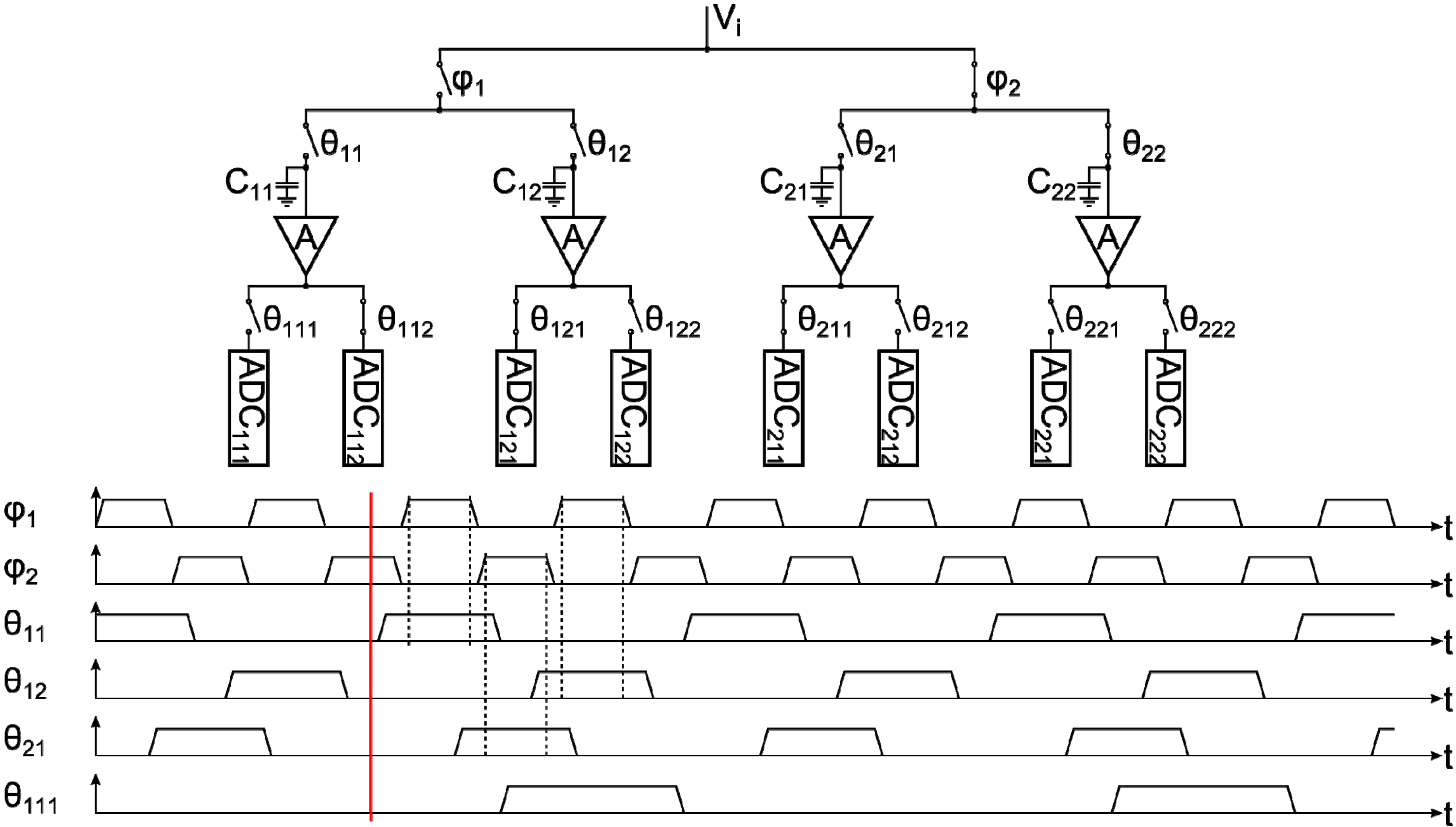
Final interleaver

- Combine sub-sampling with inline demux
- Inline demux reduces bandwidth
- Approx. 120ps hold time sufficient
- Optimize N and M of inline demux for max. bandwidth
  → N=M=P=4

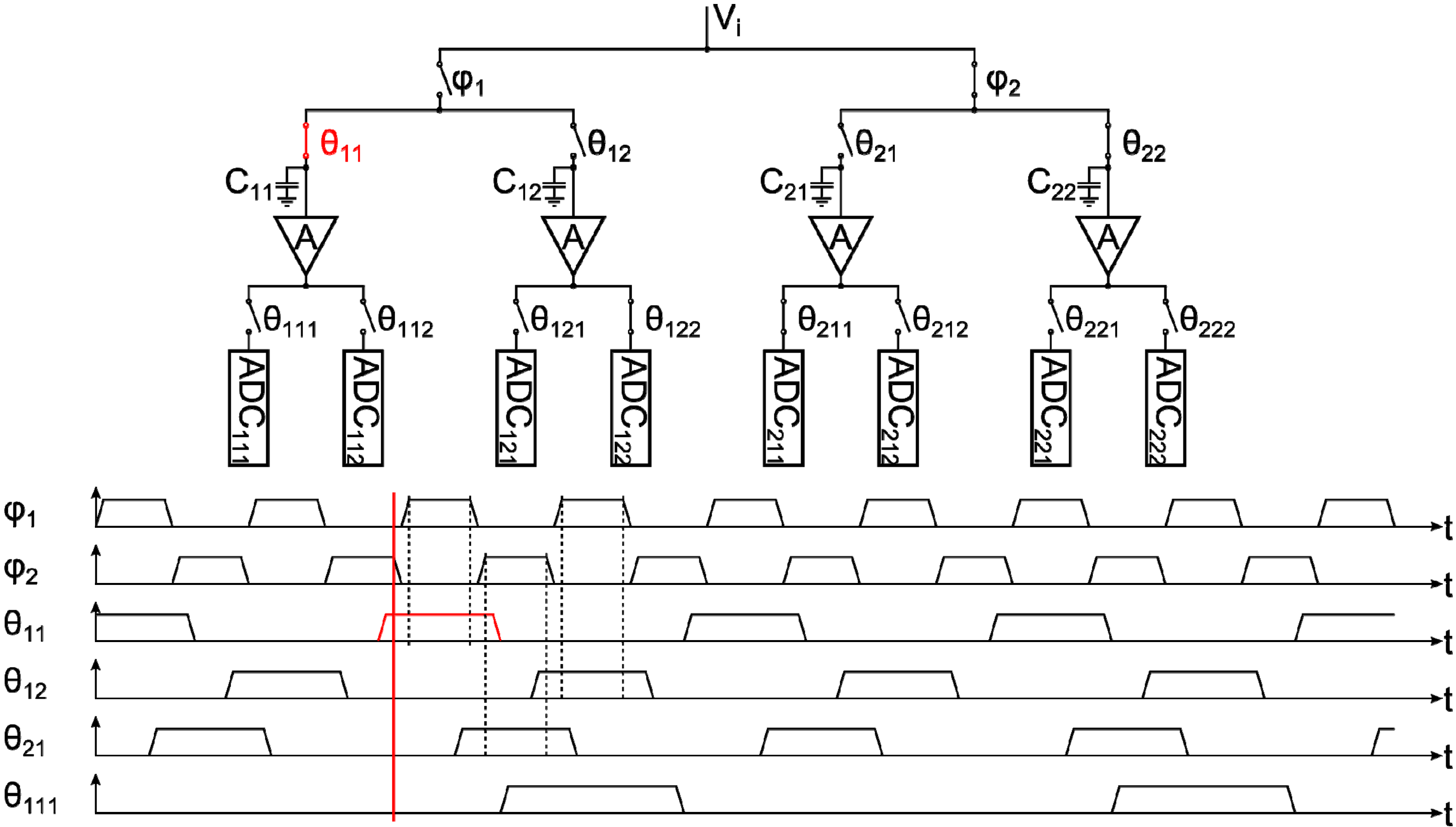
64x Interleaver



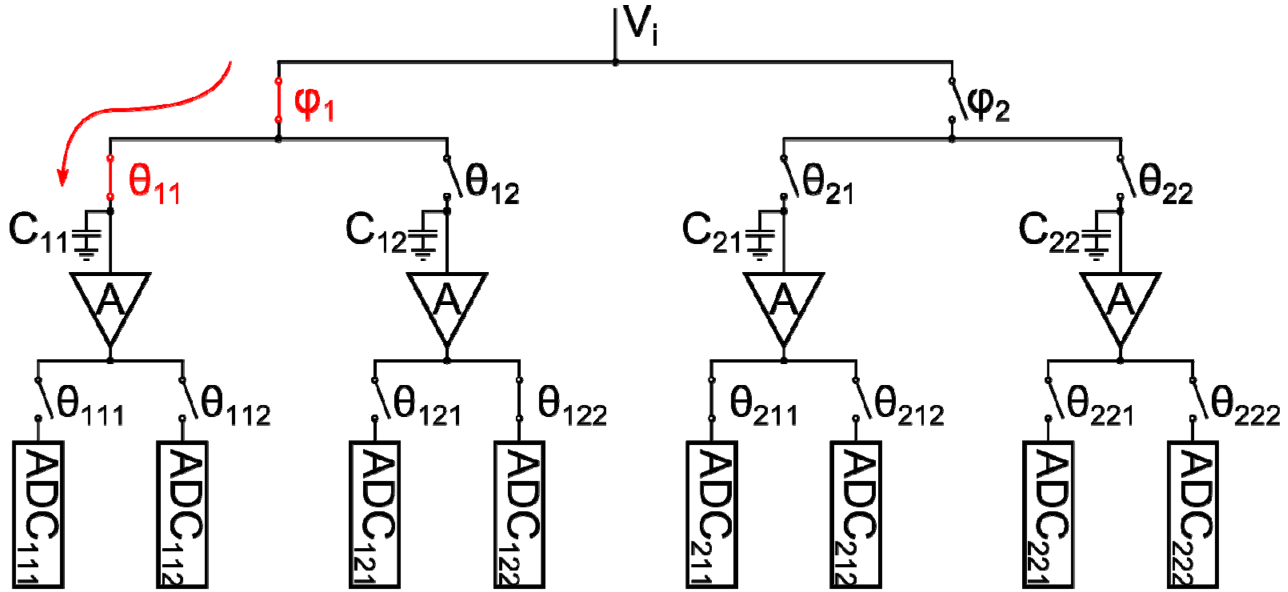
Function of the interleaver (1) (for N=M=P=2)

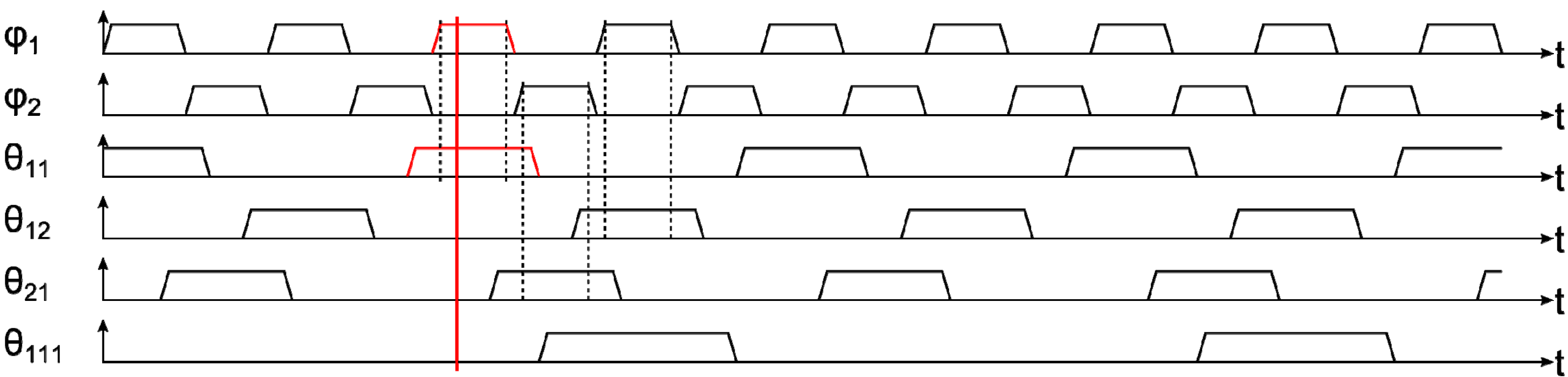


Function of the interleaver (2)

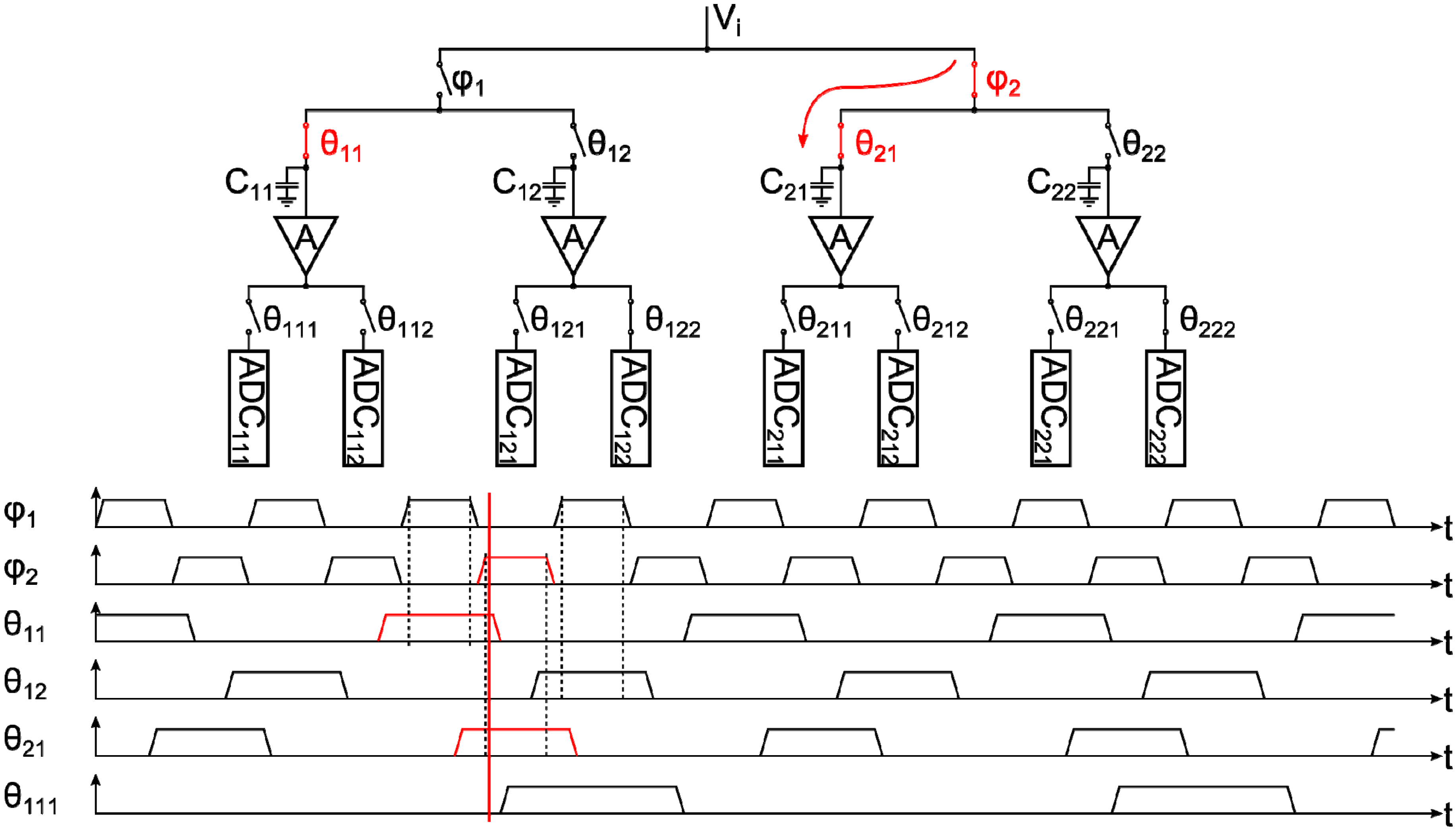


Function of the interleaver (3)

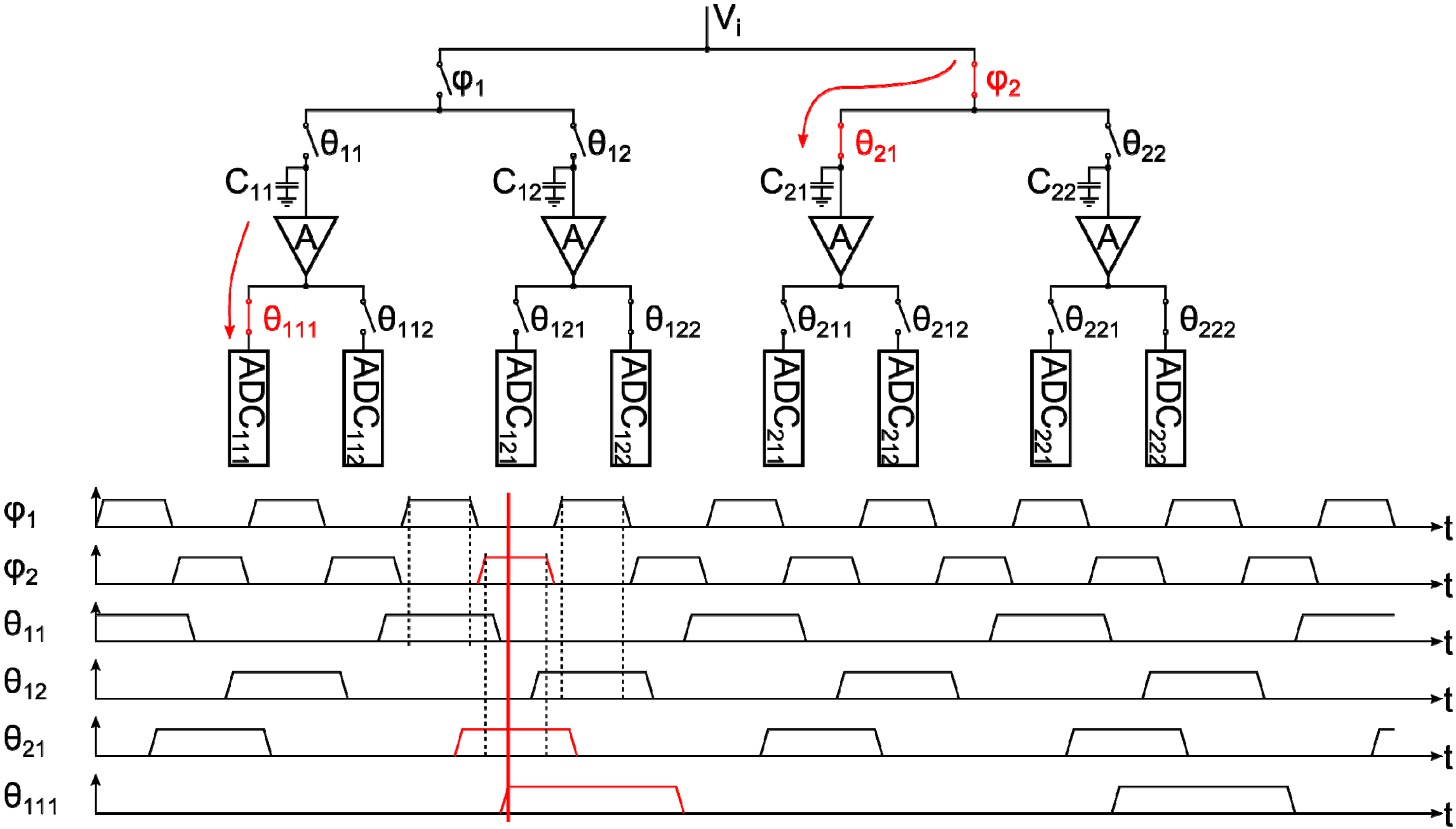




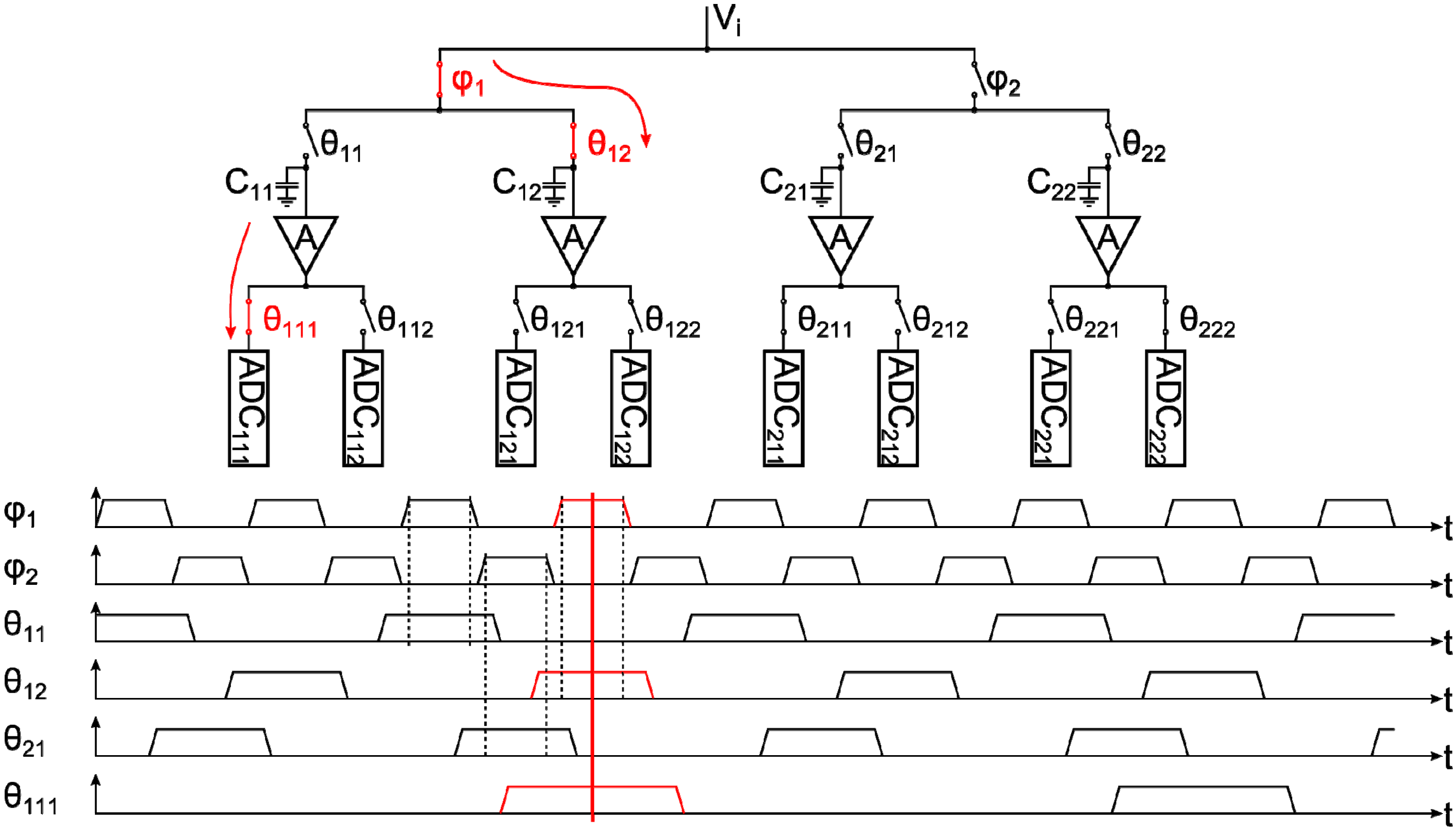
Function of the interleaver (4)



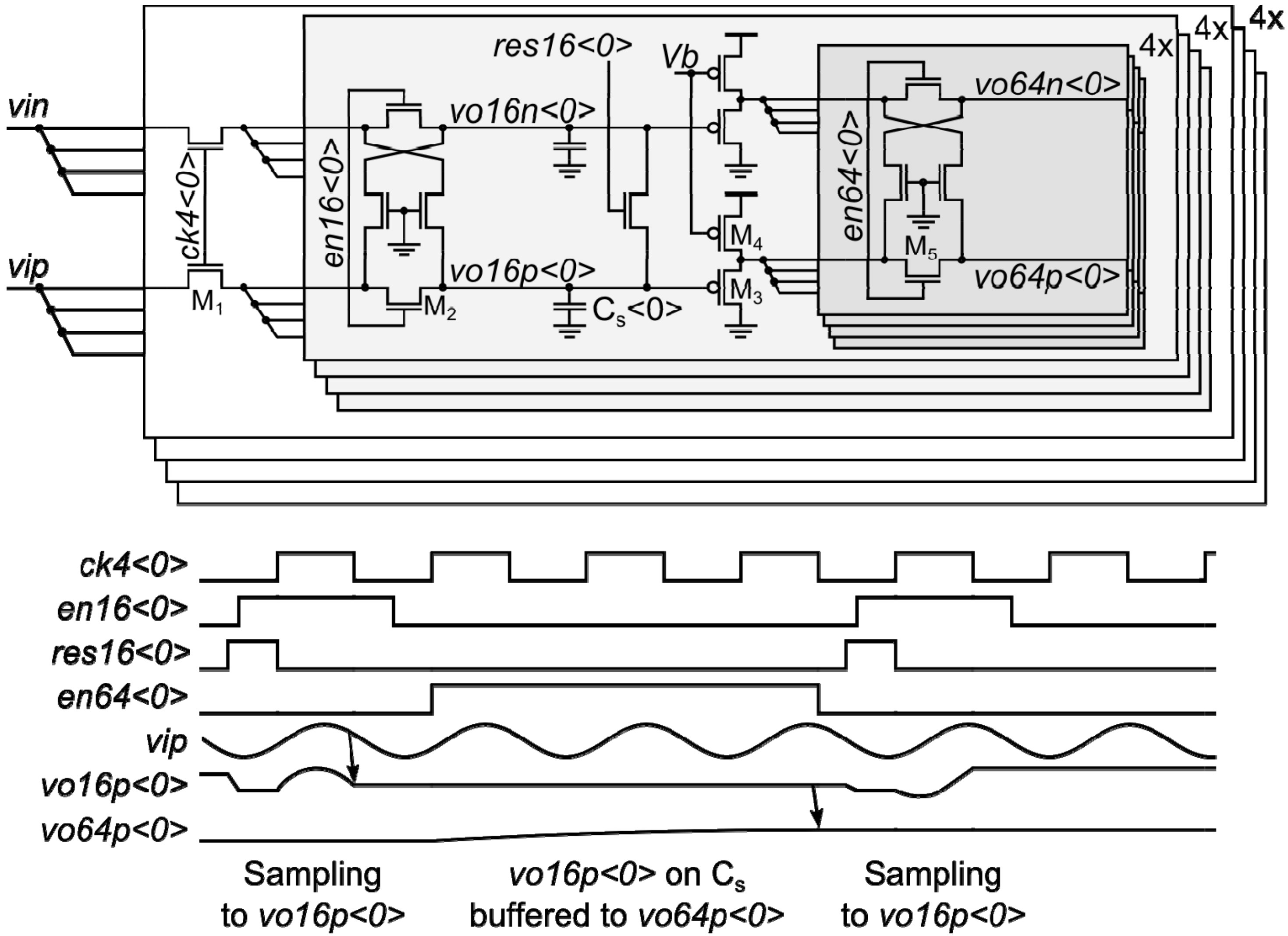
Function of the interleaver (5)



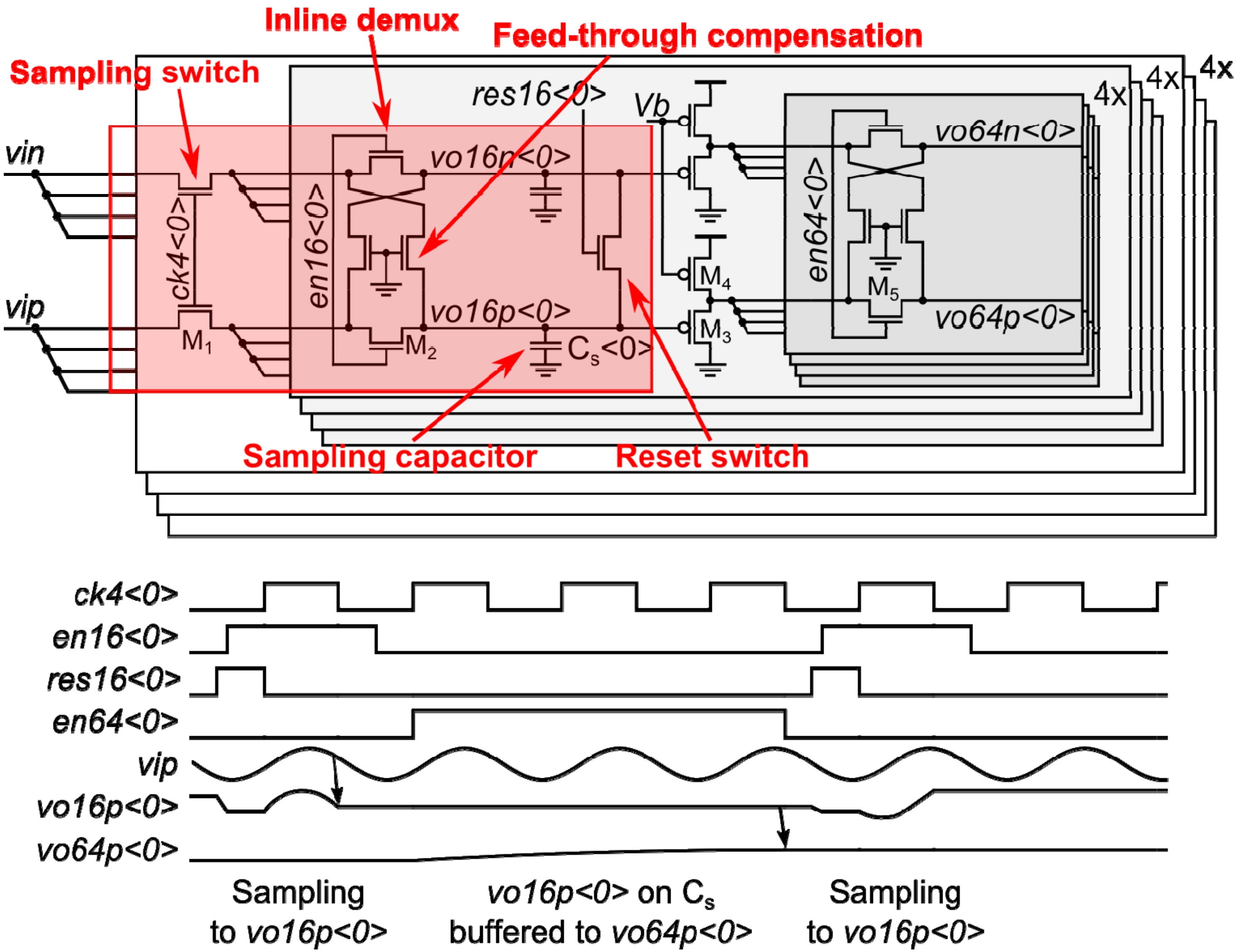
Function of the interleaver (6)



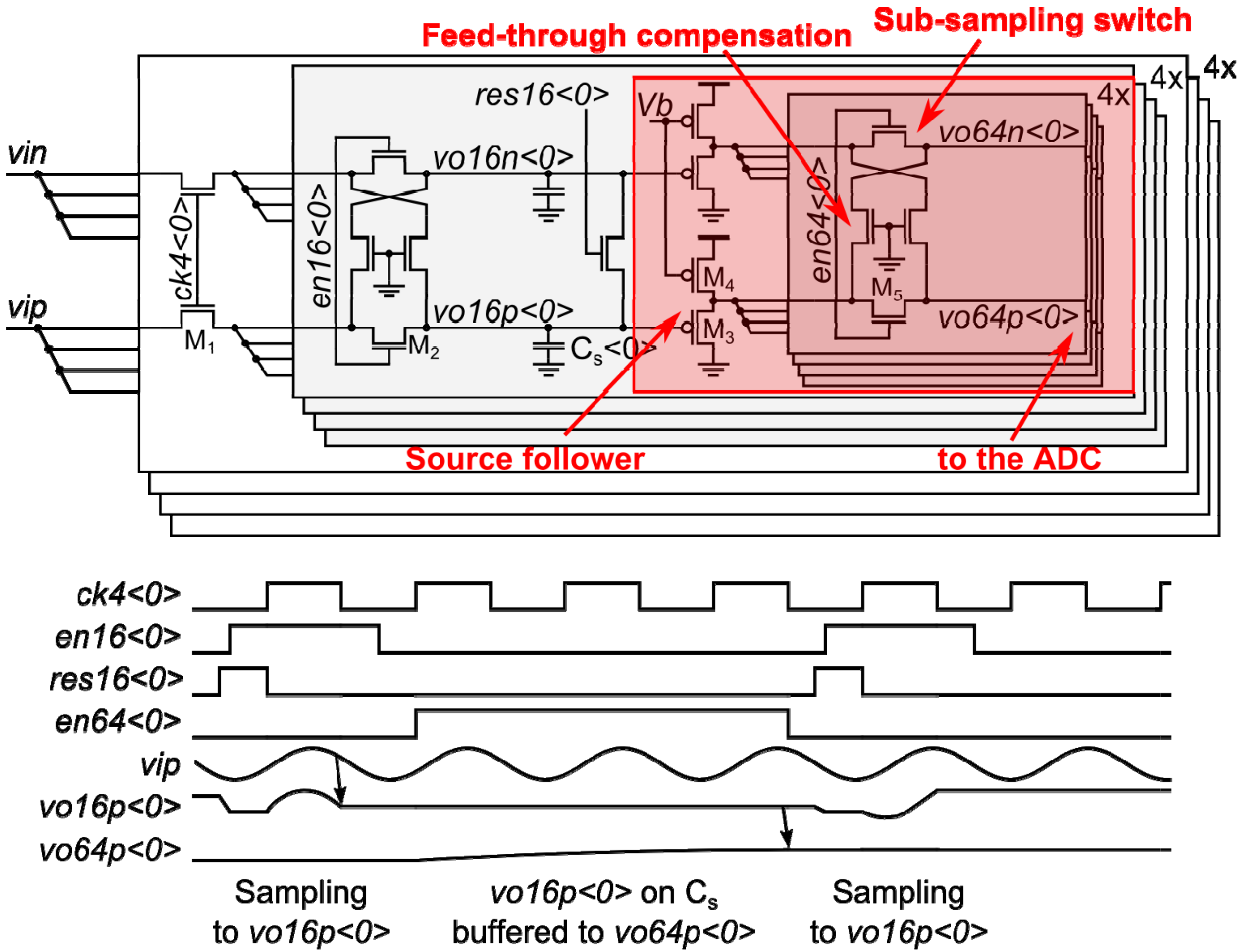
Implementation of the interleaver



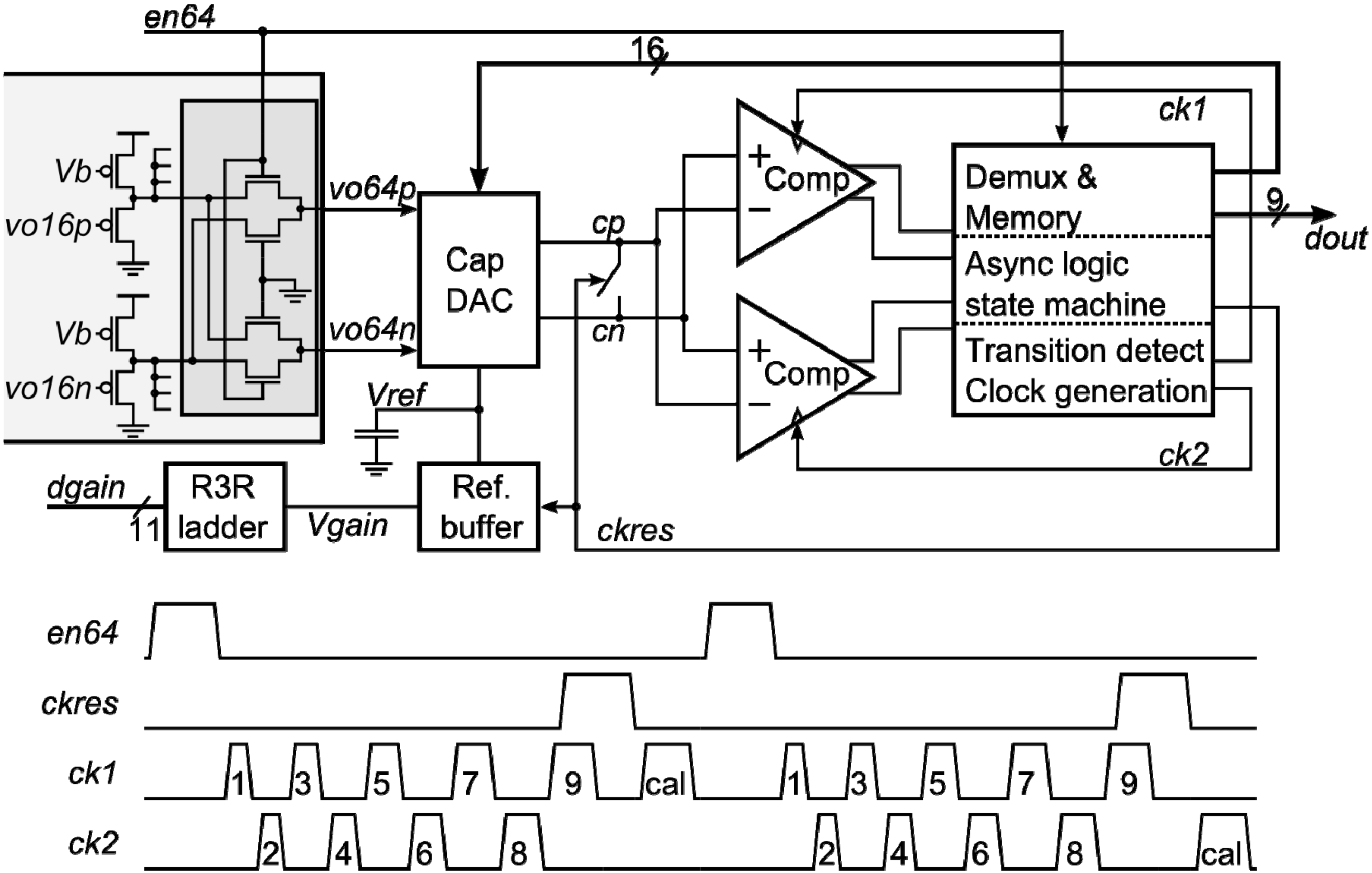
Interleaver: inline demux sampling



Interleaver: sub-sampling



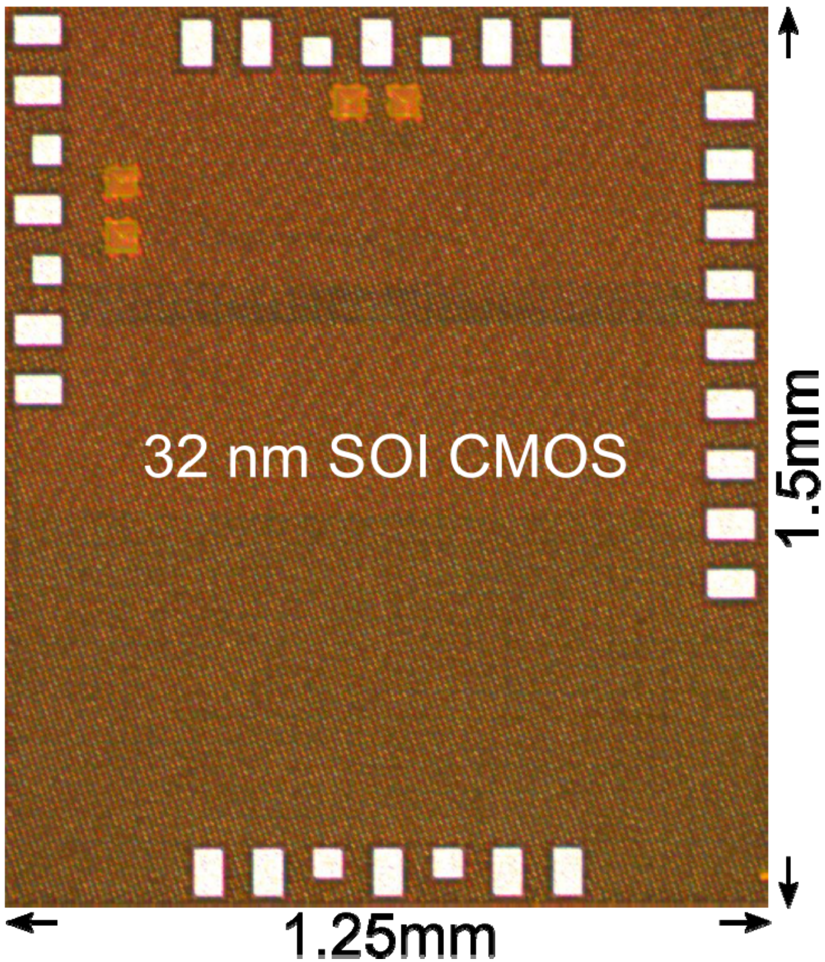
Sub-ADC

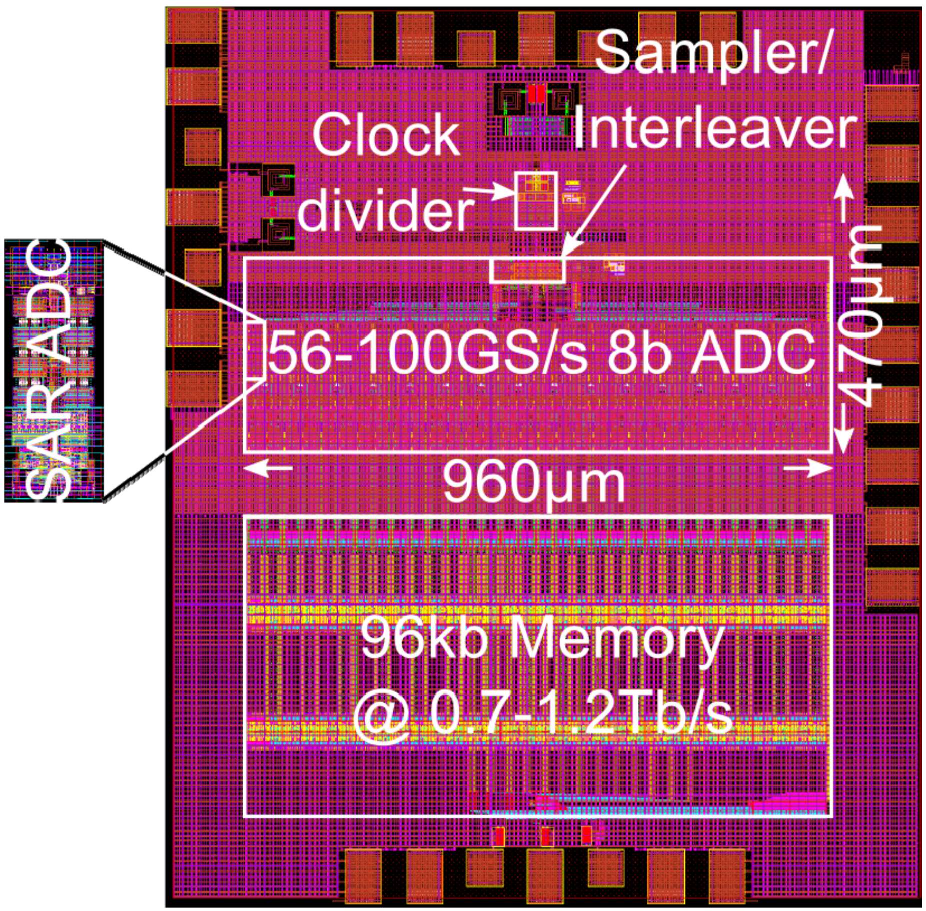

en64
16
ck1
Vb
vo16p
Vb
vo16n
vo64p
vo64n
Cap
DAC
cp
cn
Comp
Comp
Demux &
Memory
Async logic
state machine
Transition detect
Clock generation
9
dout
Vref
ck2
dgain
11
R3R
ladder
Vgain
Ref.
buffer
ckres
en64
ckres
ck1
1 3 5 7 9 cal 1 3 5 7 9
ck2
2 4 6 8 2 4 6 8 cal

Calibration

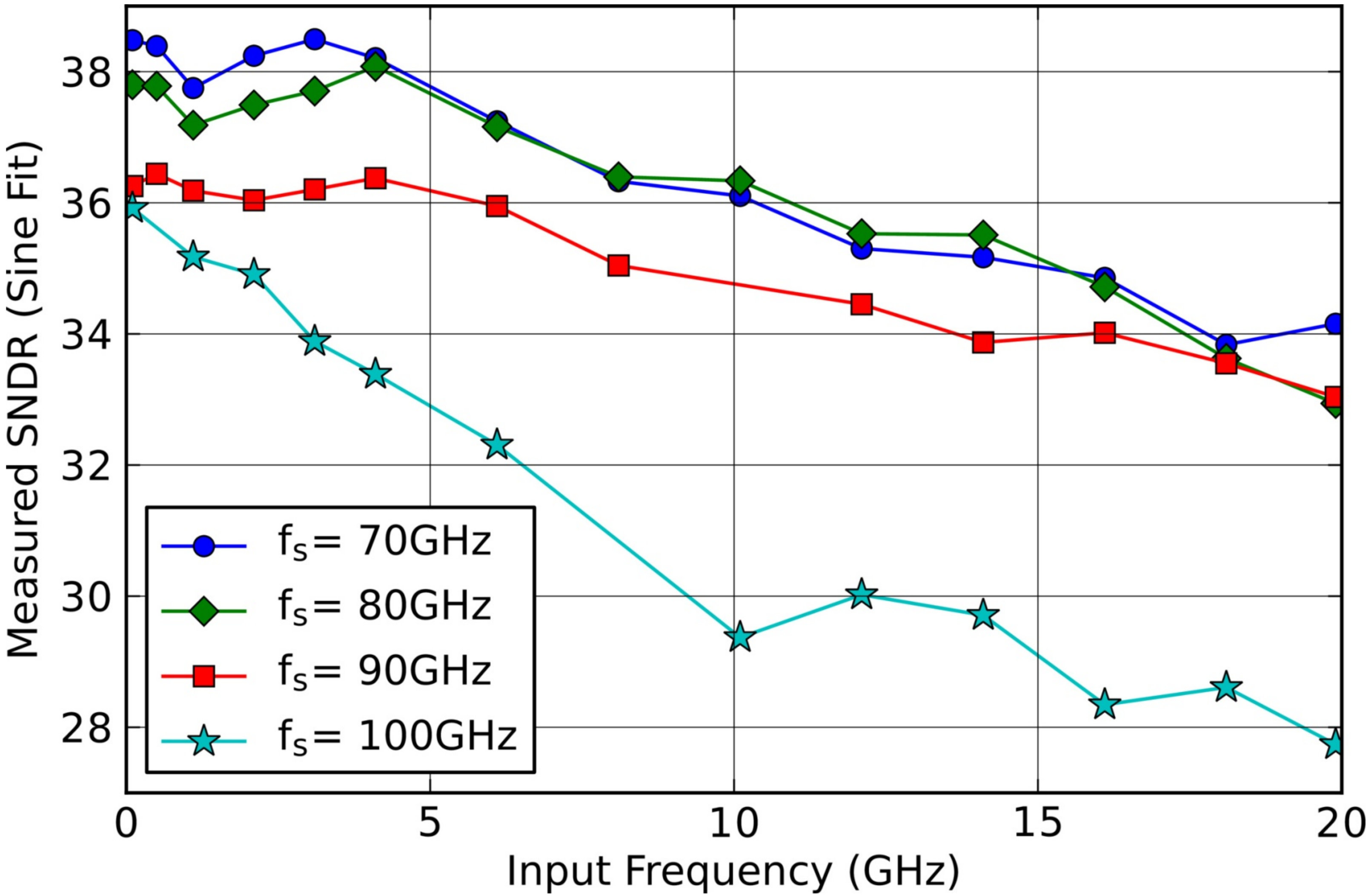
- Offset
  - Auto-zero inside SAR
  - Offline between SARs (1 point cal)
- Gain
  - On chip adjustment from off-chip sine-fit analysis (1 point cal)
  - Adjusted with SAR reference voltages
- Skew
  - On chip adjustment from off-chip sine-fit analysis (1 point cal)
  - Adjusted in clock divider before sampling switches
- Bandwidth
  - No calibration

Die Photo

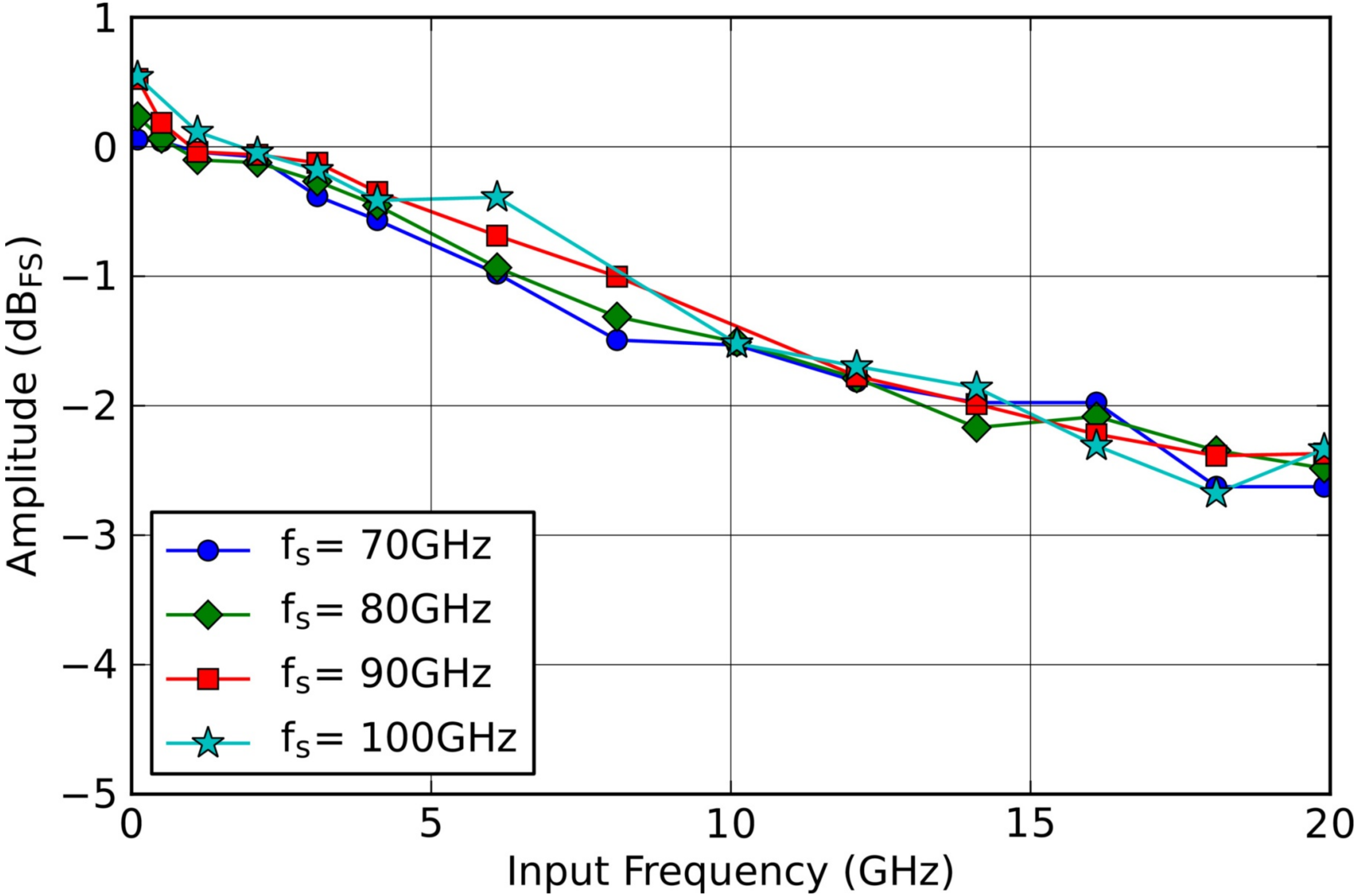

32 nm SOI CMOS
1.5mm
1.25mm


SAR ADC
Sampler/
Interleaver
Clock
divider
56-100GS/s 8b ADC
470µm
960µm
96kb Memory
@ 0.7-1.2Tb/s

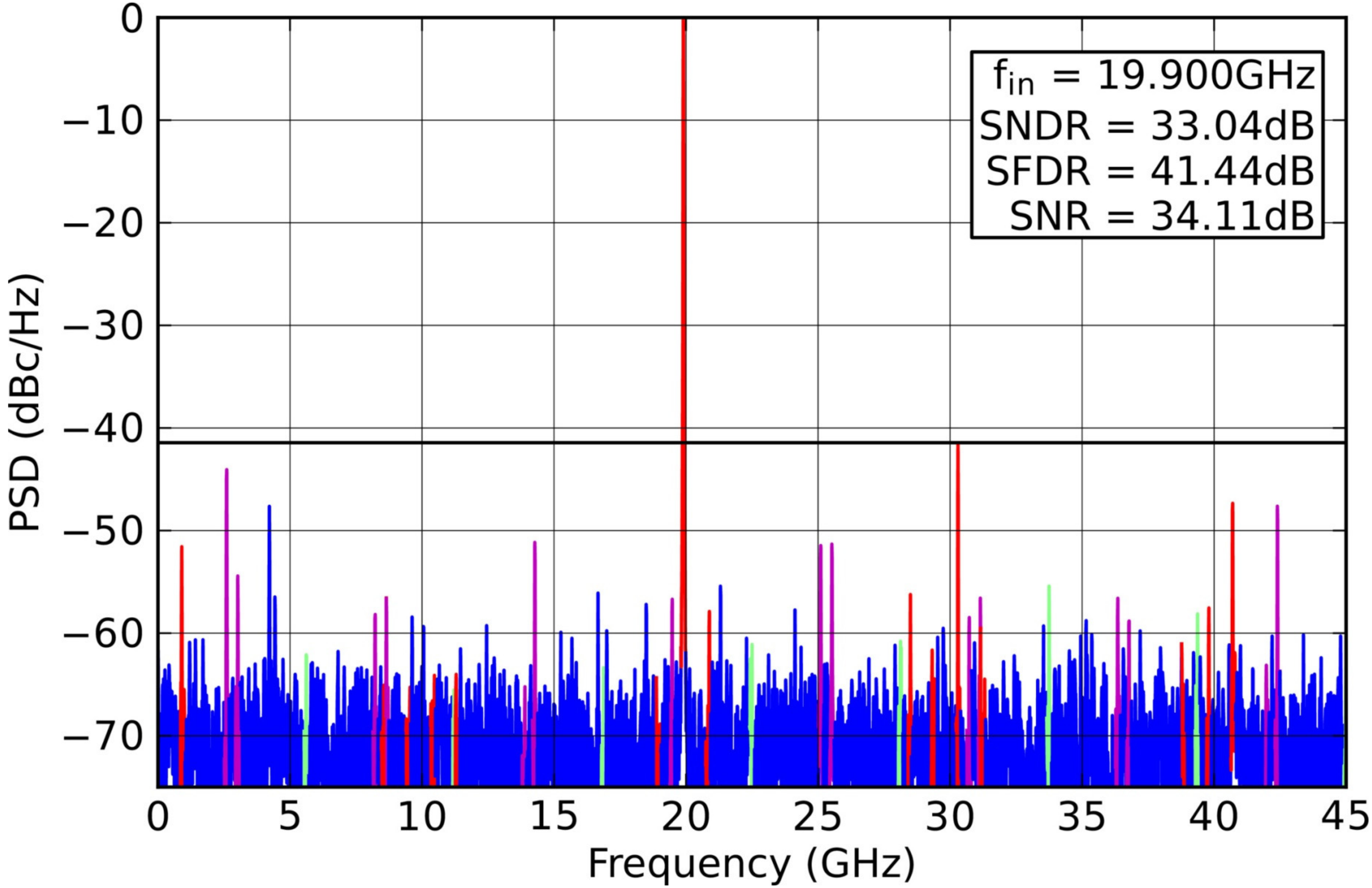
SNDR vs. input frequency



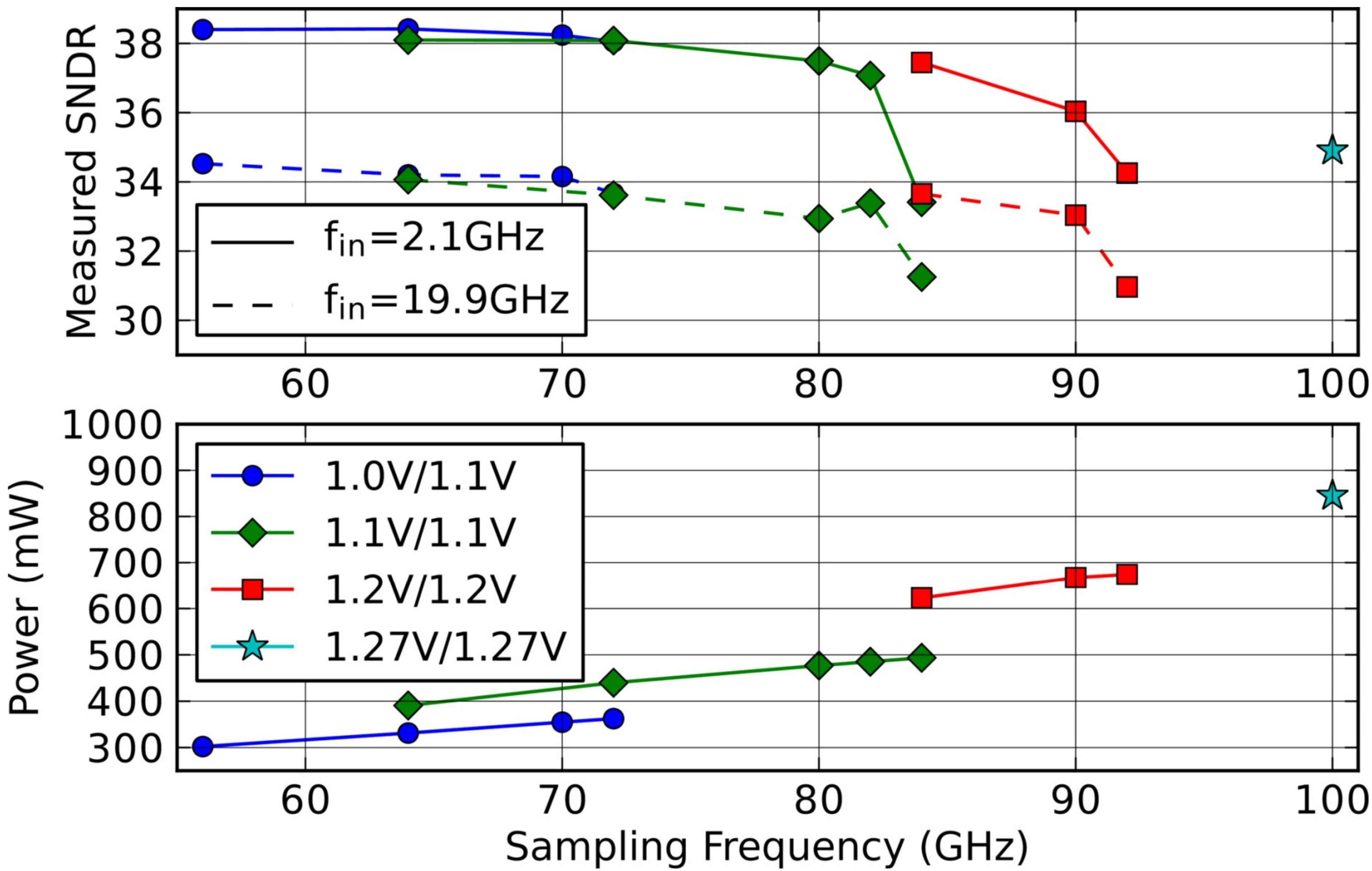
Amplitude vs. input frequency



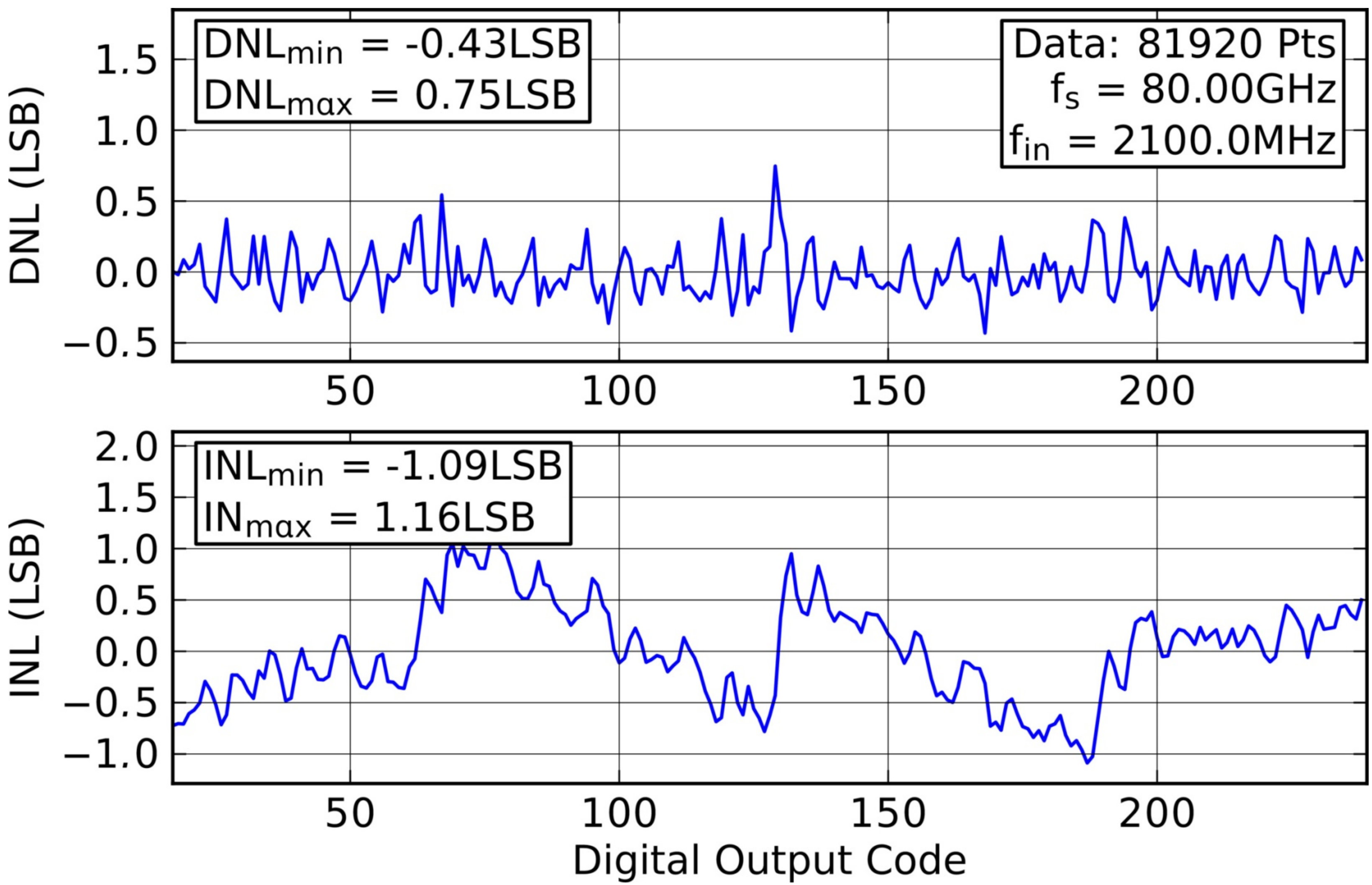
Frequency Spectrum



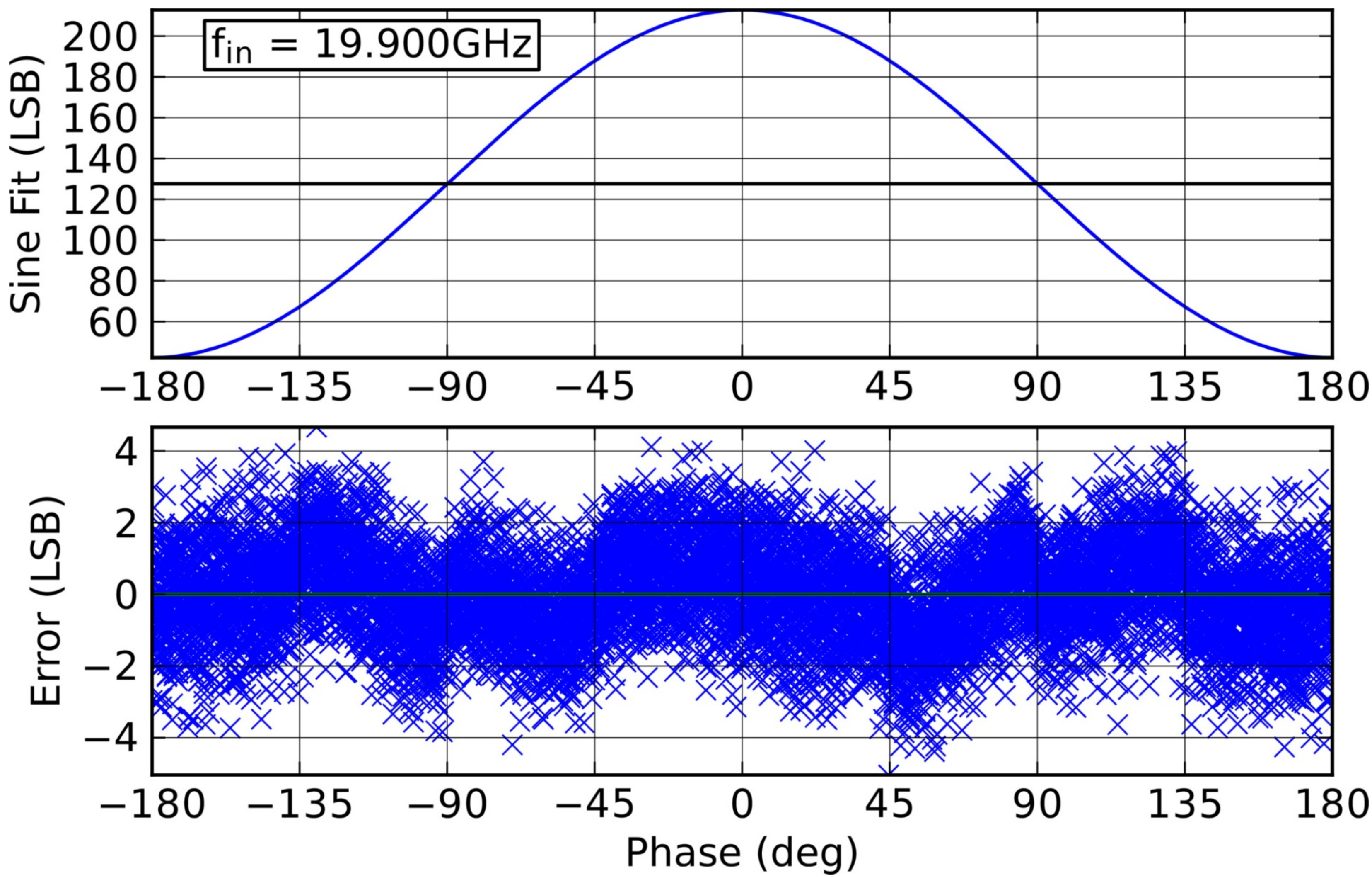
SNDR and power vs. sampling frequency



INL and DNL


DNLmin = -0.43LSB
DNLmax = 0.75LSB
Data: 81920 Pts
fs = 80.00GHz
fin = 2100.0MHz
DNL (LSB)
1.5
1.0
0.5
0.0
−0.5
50
100
150
200
INLmin = -1.09LSB
INmax = 1.16LSB
INL (LSB)
2.0
1.5
1.0
0.5
0.0
−0.5
−1.0
50
100
150
200
Digital Output Code

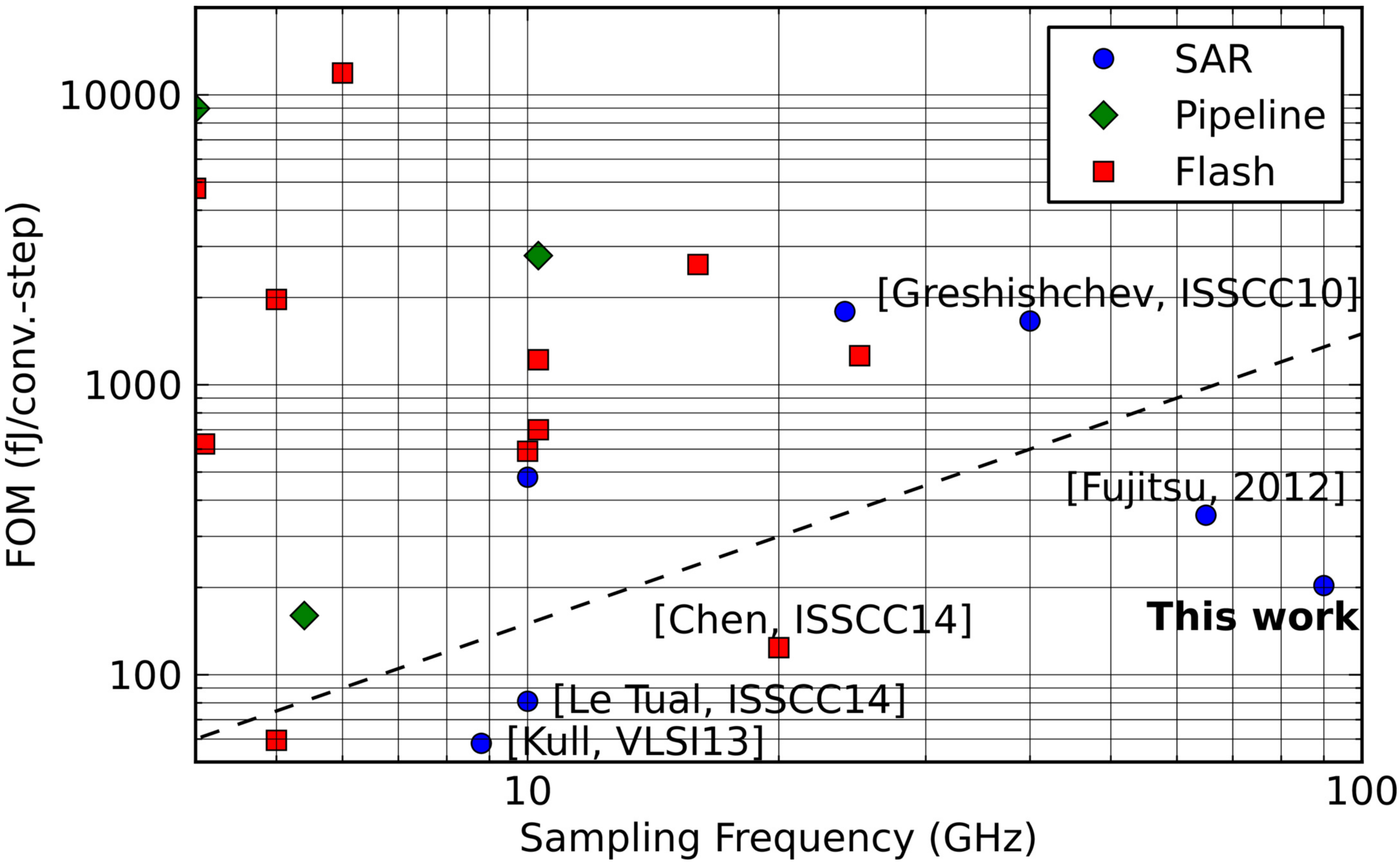
Modulo-time plot



Performance summary

Technology	32nm SOI CMOS			
Architecture	TI-SAR			
Resolution	8			
Sampling speed (GHz)	70	80	90	100
Supply V_{DA}/V_{DI} (V)	1.0/1.1	1.1	1.2	1.27
Input range ($V_{pp\text{-}diff}$)	0.7	0.7	0.8	0.85
SNDR (0-6.1GHz) (dB)	37.7	37.2	36.0	34.9
SNDR (0-19.9GHz) (dB)	34.2	32.9	33.0	27.7
3dB bandwidth (GHz)		22		
Power (mW)	355	477	667	845
FOM (0-6.1GHz) (fJ/conv. step)	81	101	144	186
FOM (0-19.9GHz) (fJ/conv. step)	121	165	203	426
Area (mm^2)	0.45			

ADC performance plot: FOM



Conclusion

- Interleaver:
  - Combination of sub-sampling and inline demux
  - Only 4 critical clocks
- 90 GS/s ADC:
  - 50% faster than previous CMOS ADCs
  - 50% lower FOM*
  - Measured up to 100 GS/s

→Fastest CMOS ADC at best energy efficiency and lowest area*

* Compared to ADCs with 6b+, >20GS/s

A 69.5mW 20GS/s 6b Time-Interleaved ADC with Embedded Time-to-Digital Calibration in 32nm CMOS SOI

Vanessa Hung-Chu Chen and Lawrence Pileggi

Carnegie Mellon University

Outline

- Motivation
- Calibration Algorithms
  - ❖ Gain and Offset Calibration
  - ❖ Embedded Time-to-Digital Calibration
- Circuit Implantation
- Measurement Results
- Conclusions

Motivation

- 8-way flash ADCs interleaved in time to achieve 20GS/s for wireline communication systems
- Near minimum size transistors in comparators and buffers
- No full rate clock & 2-rank T/H
- Process mismatch is transformed into dynamic errors
- Timing skew of < 200 fs_{rms} is required to achieve 6b resolution for a 10GHz input

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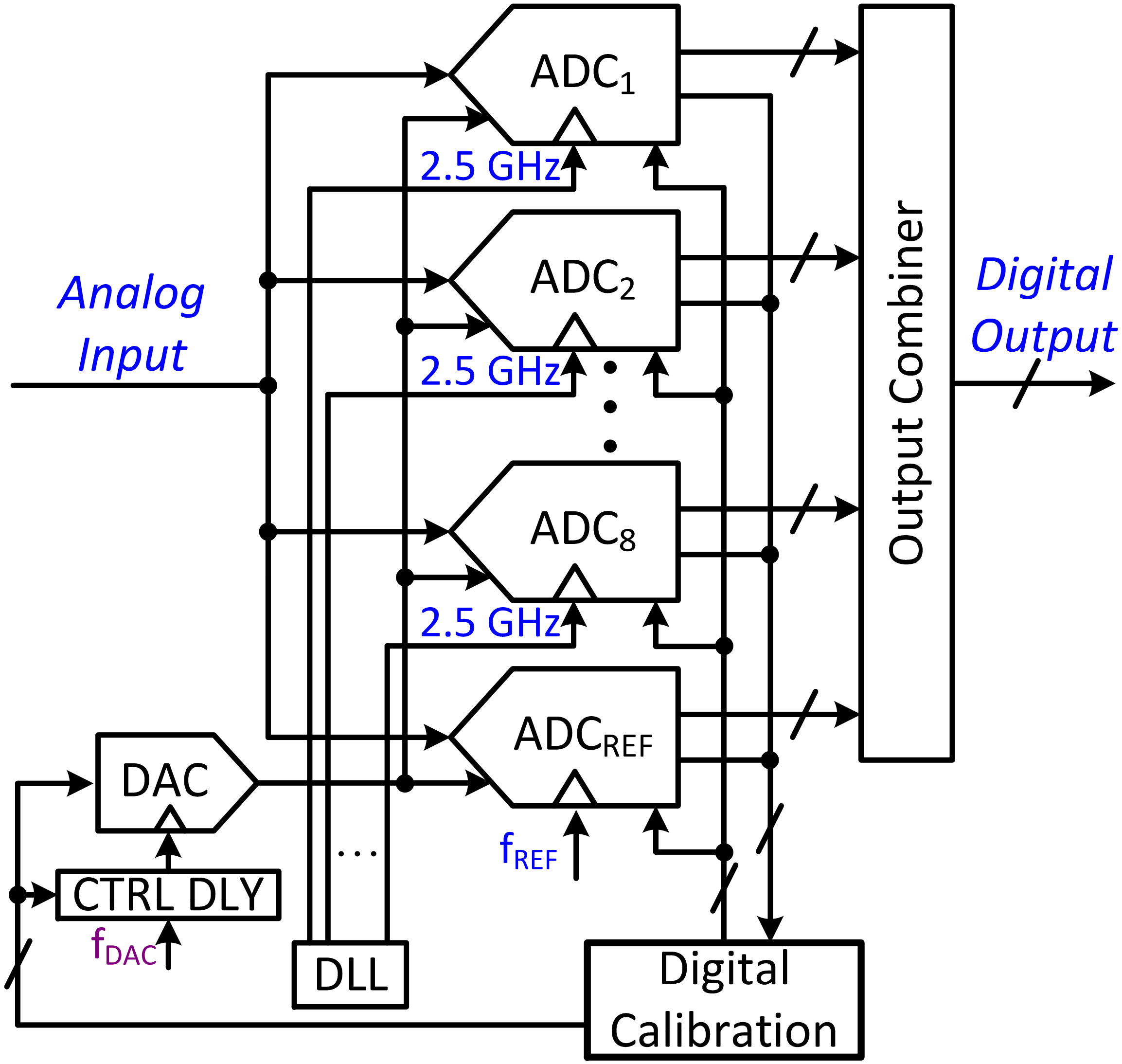
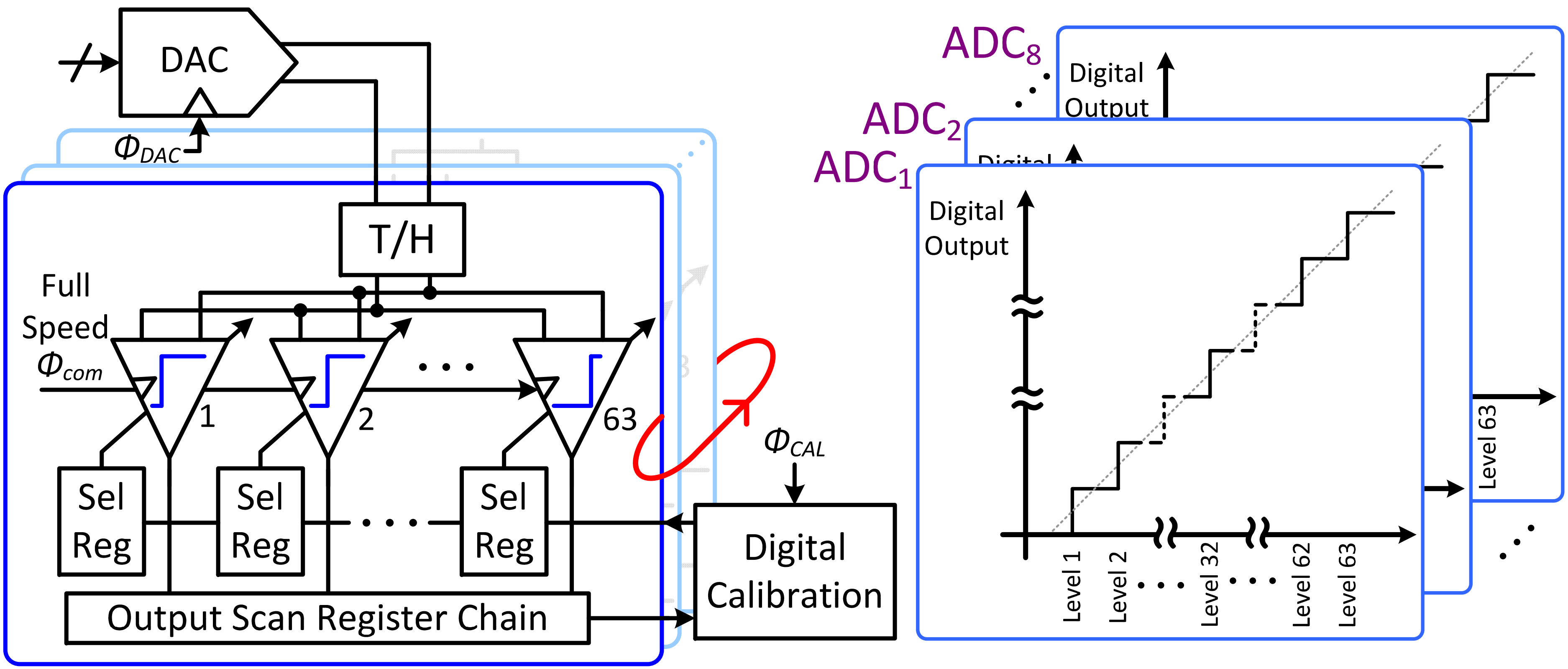
ADC Architecture

- 8 sub-ADCs + ADC_{REF}
- DLL generates 8 phases
- Digital logics & DAC w/ delay line for background Calibration



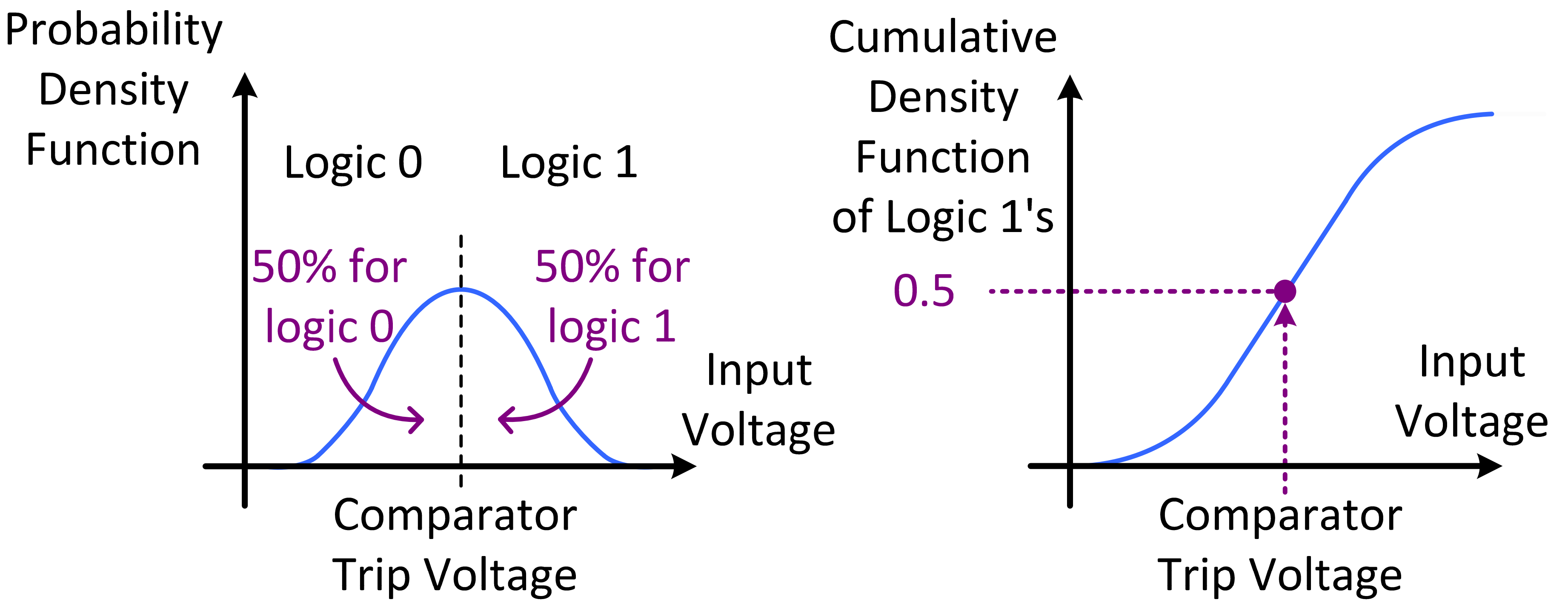
Inter-Channel Mismatch Calibration

- Each sub-ADC is calibrated with the DAC
  - ❖ All the transfers curve are referred to the same one



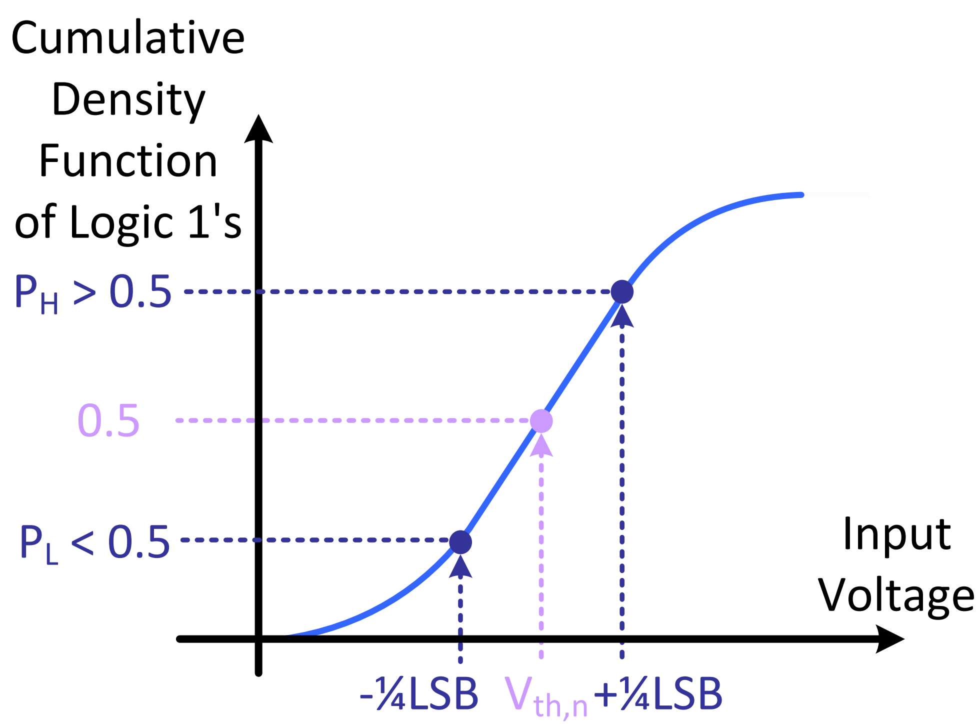
Conventional Offset Estimation

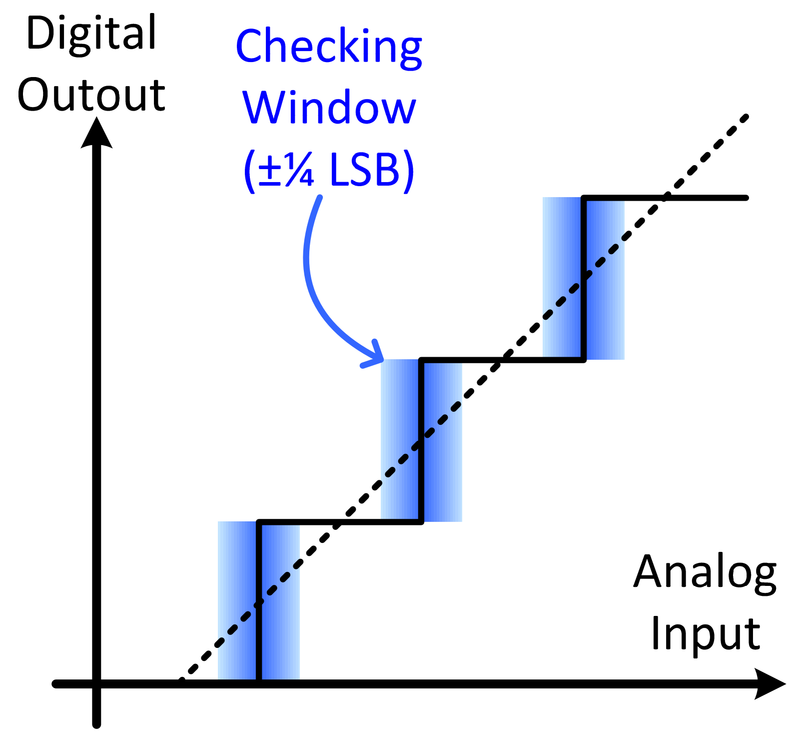
- Difficult to generate an on-chip high-linear ramp signal
- Time consuming to collect large volume of output data



Calibration Checking Window

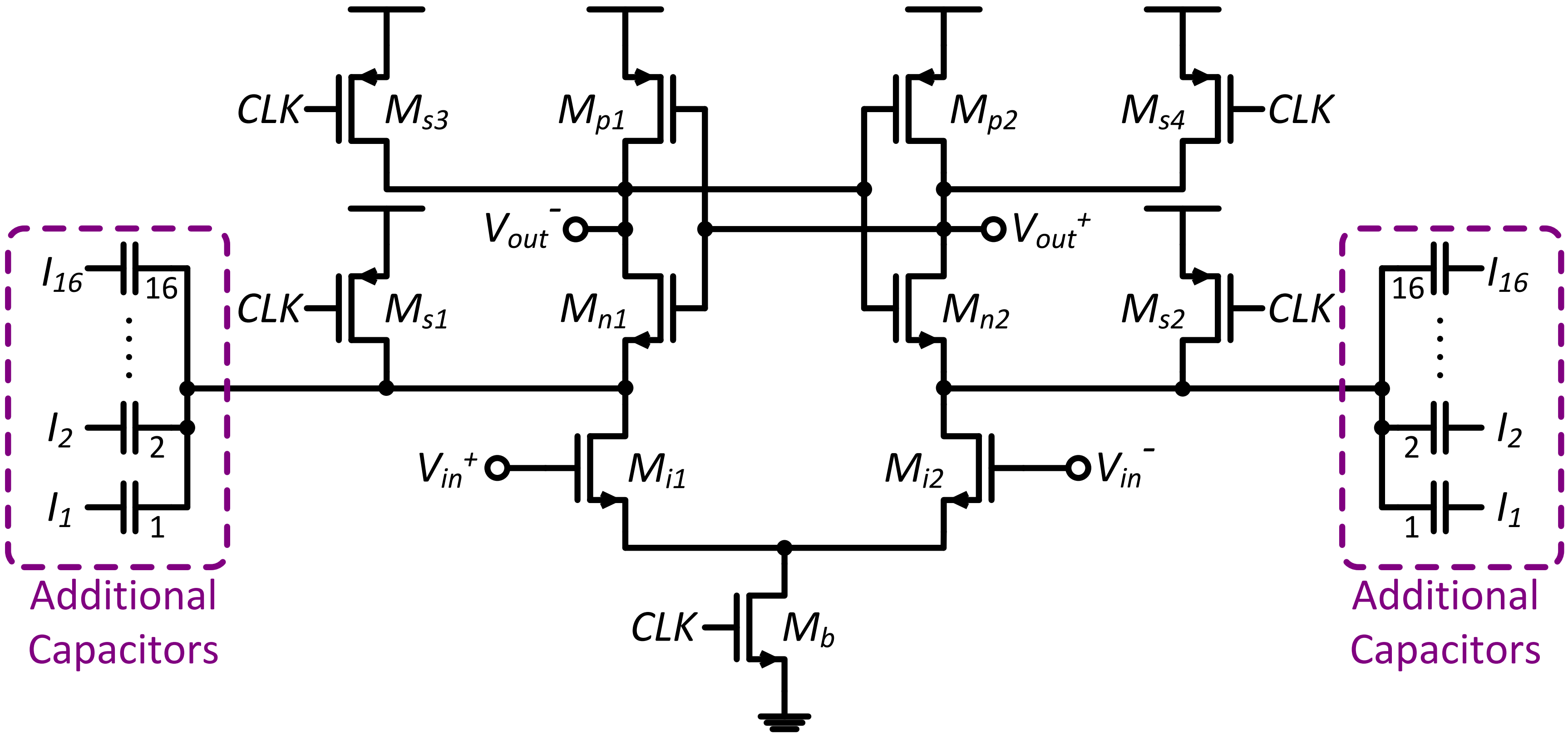
- Checking windows (±1/4 LSB) are applied
  - ❖ Only requiring 2 steps per level
  - ❖ Use a current DAC to generate 126 levels
  - ❖ Accumulators in digital domain to calculate probability





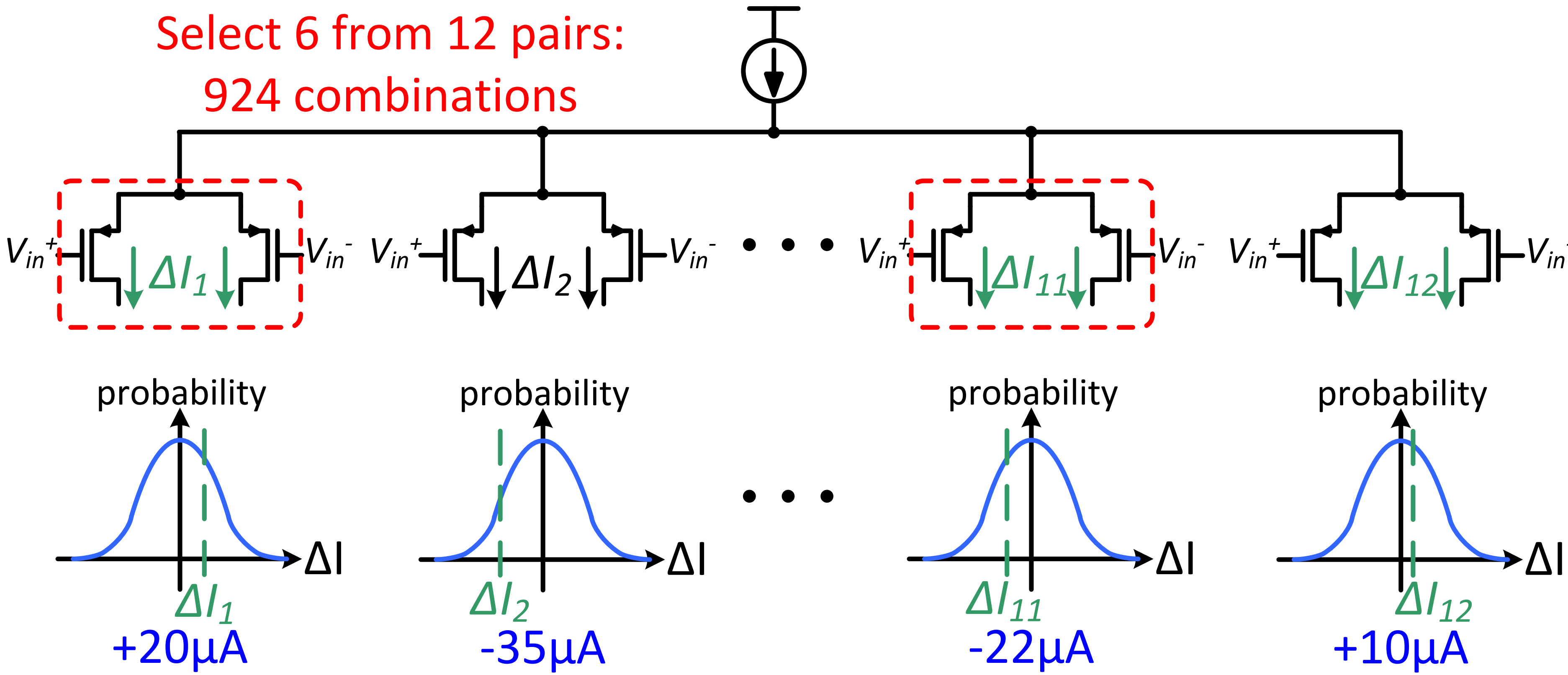
Conventional Offset Calibration

- Additional capacitors added at signal nodes
  - ❖ Slow down the operation speed ☹
  - ❖ Increase the power consumption ☹



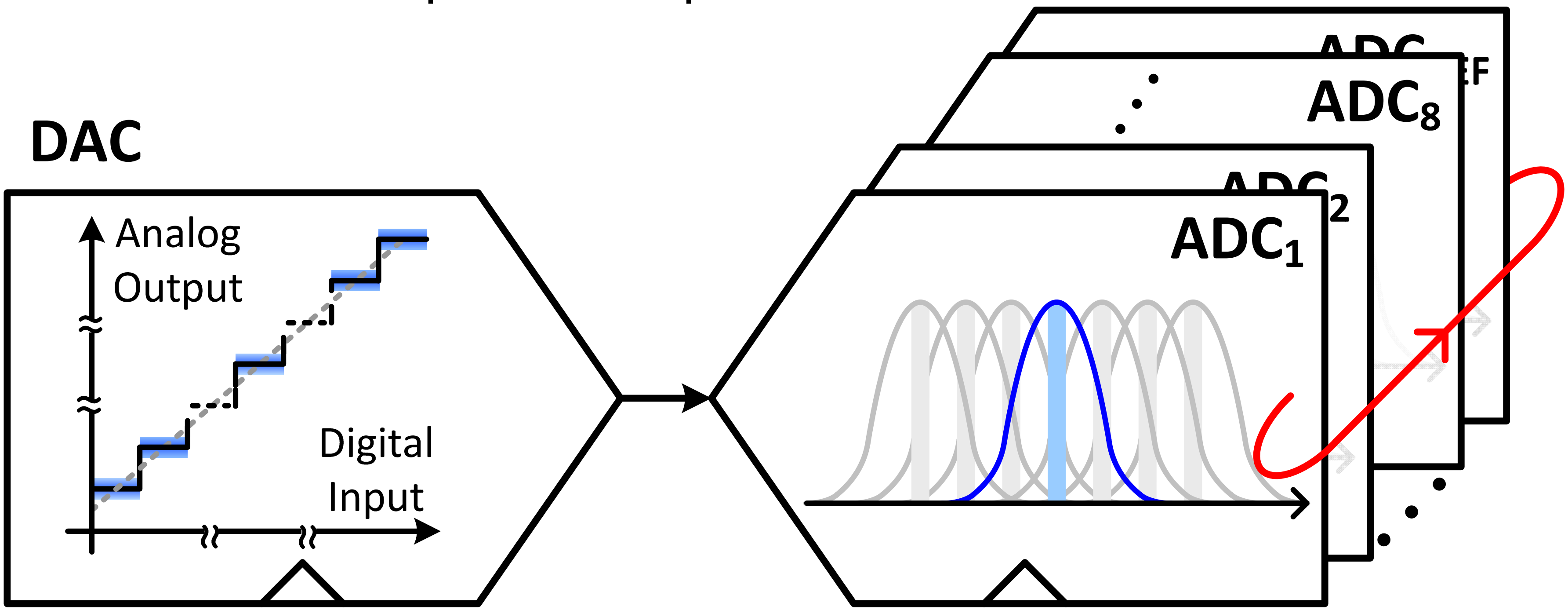
Combinatorial Differential Pair

- Exploit process randomness to compensate for mismatch



Voltage Domain Calibration

- Search a subset that finds required levels for flash ADCs
  - ❖ Apply a checking window per level
  - ❖ No extra capacitors required



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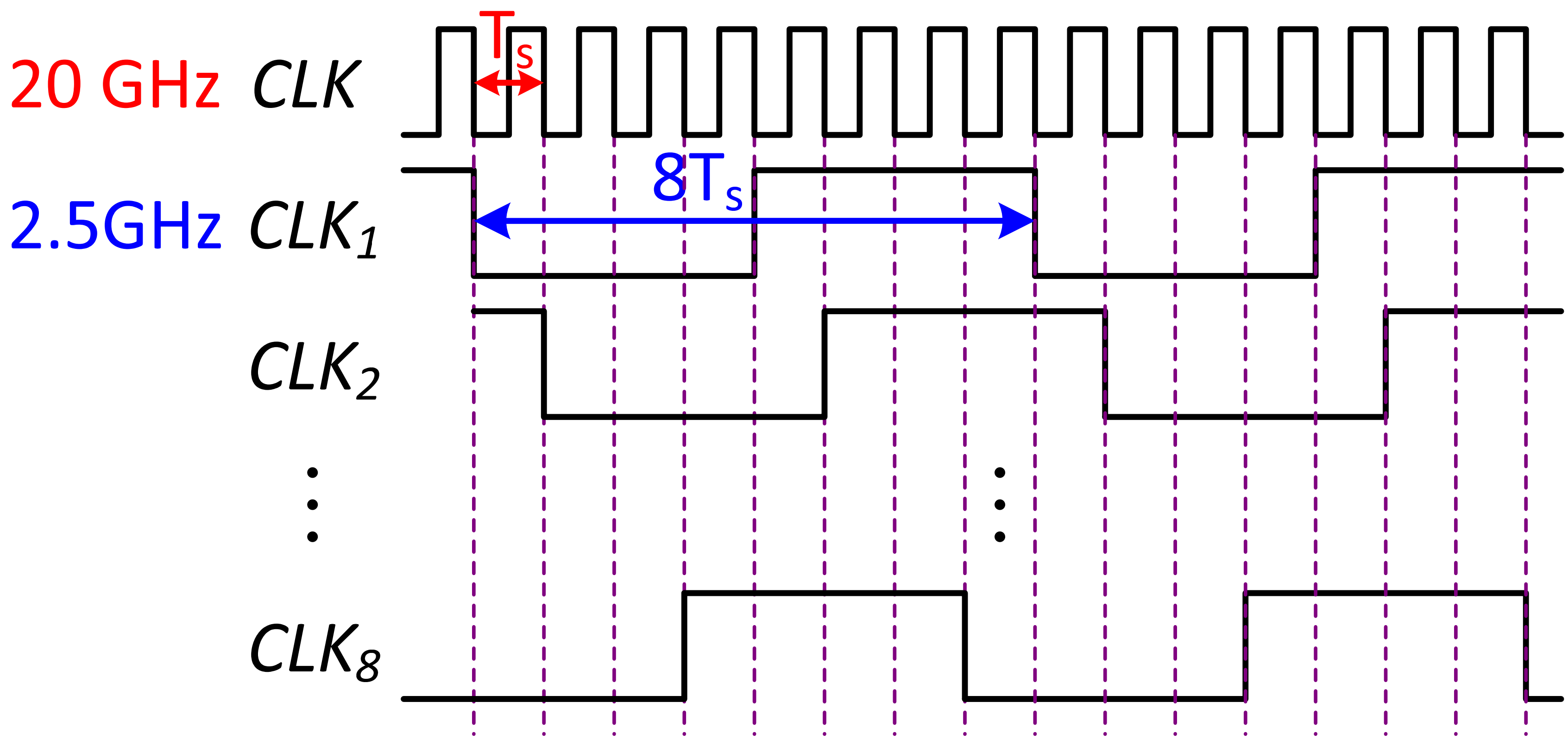
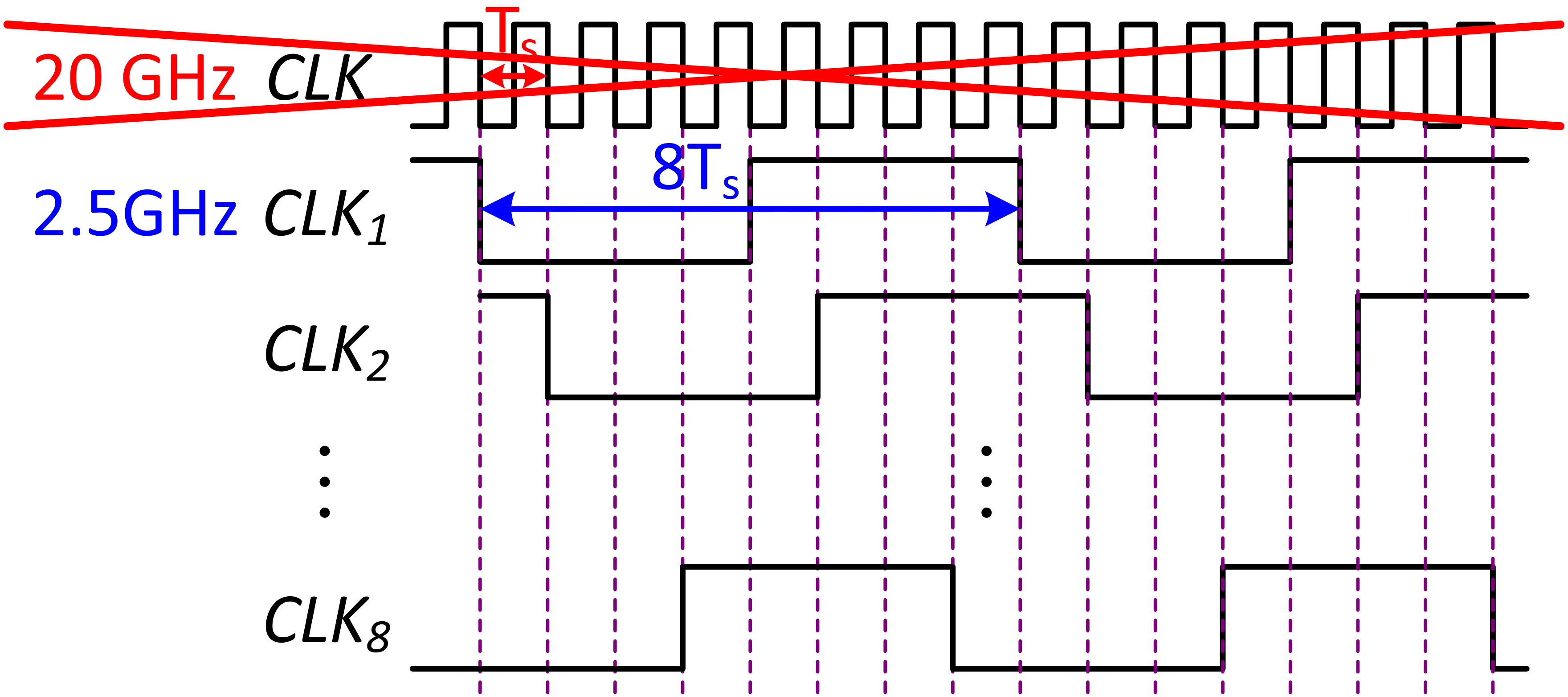
Conventional Synchronization



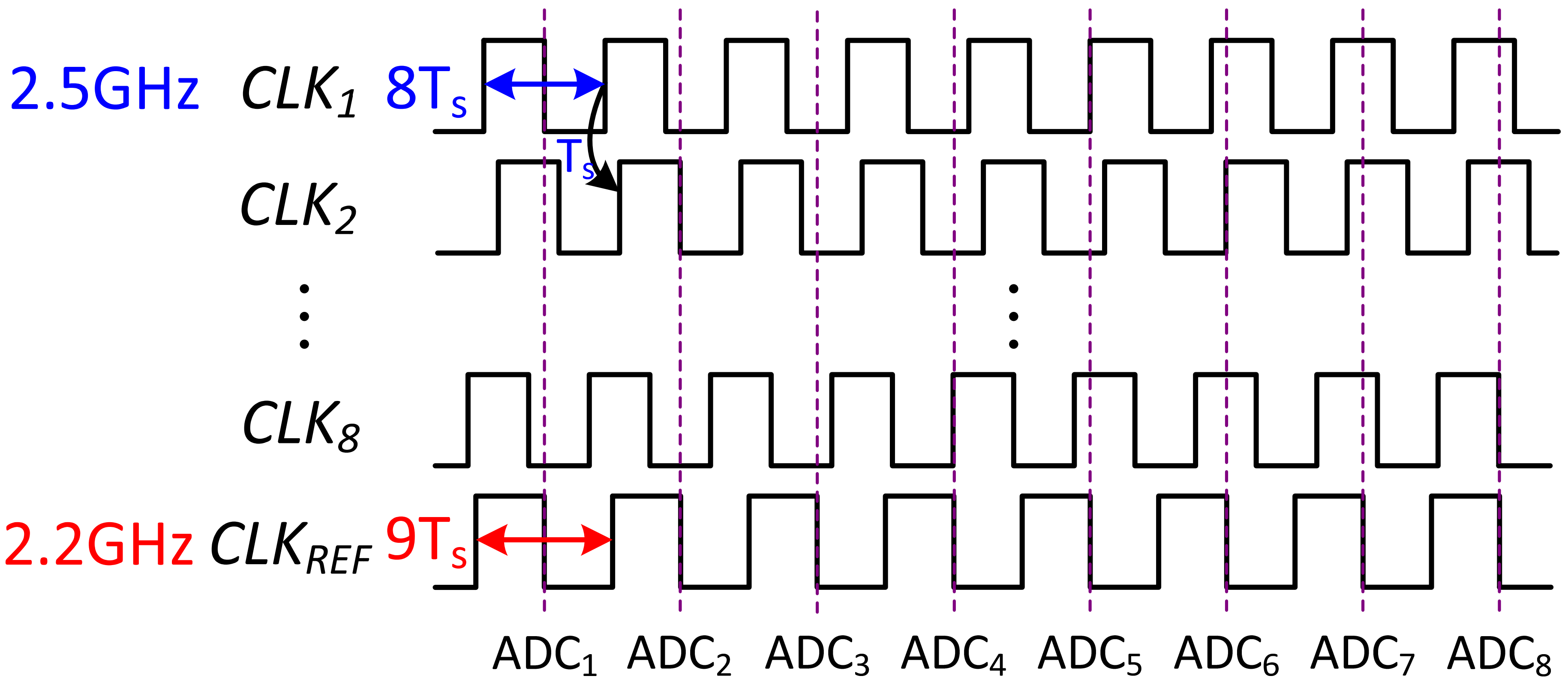
Embedded Time-to-Digital Calibration

- Avoid full rate clock to reduce power consumption



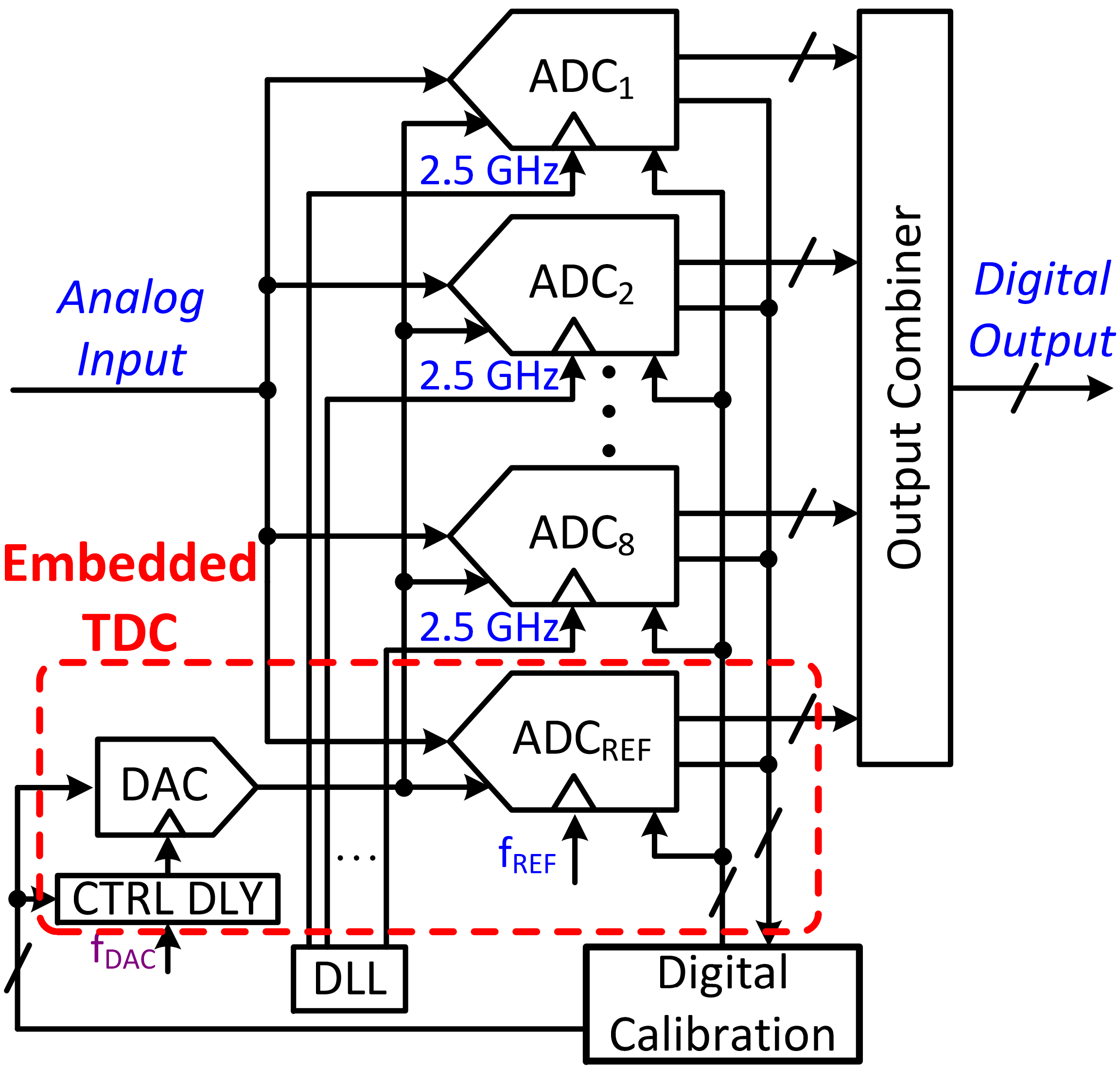
Timing Calibration

- Use a low frequency clock (2.2GHz)

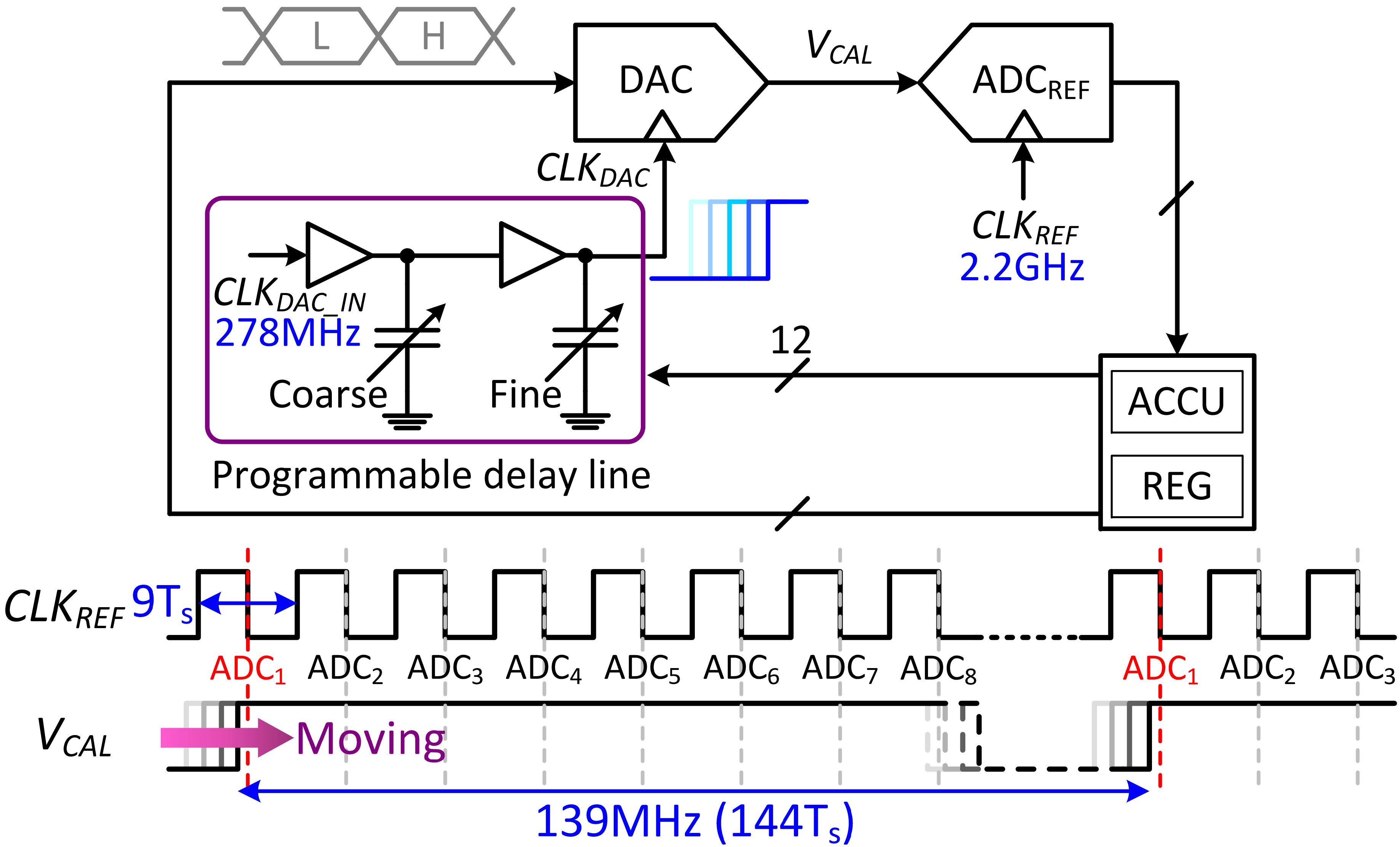


Embedded Time-to-Digital Calibration

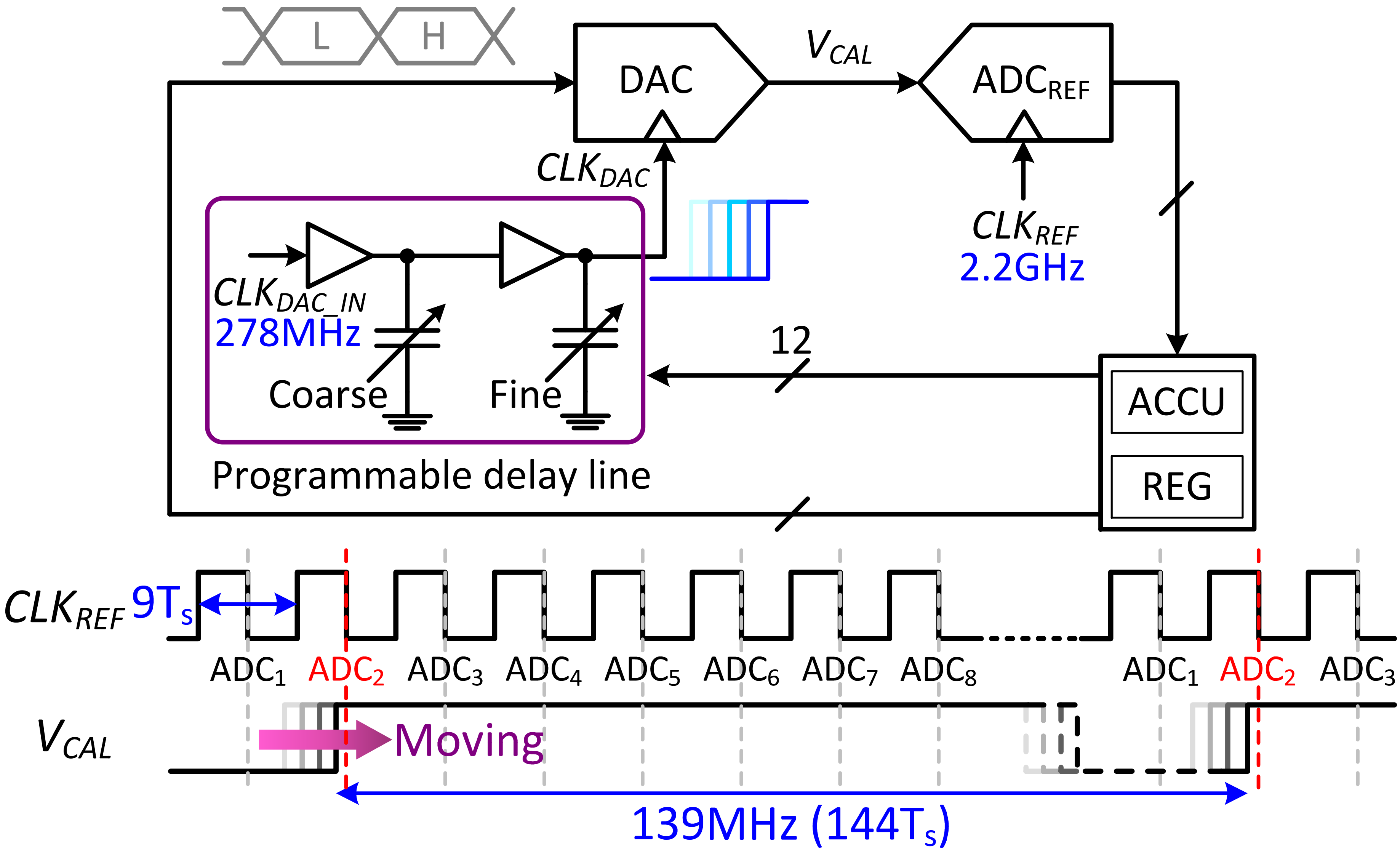
- No full rate clock (20GHz) required
- Embedded TDC: ADC and DAC with delay line



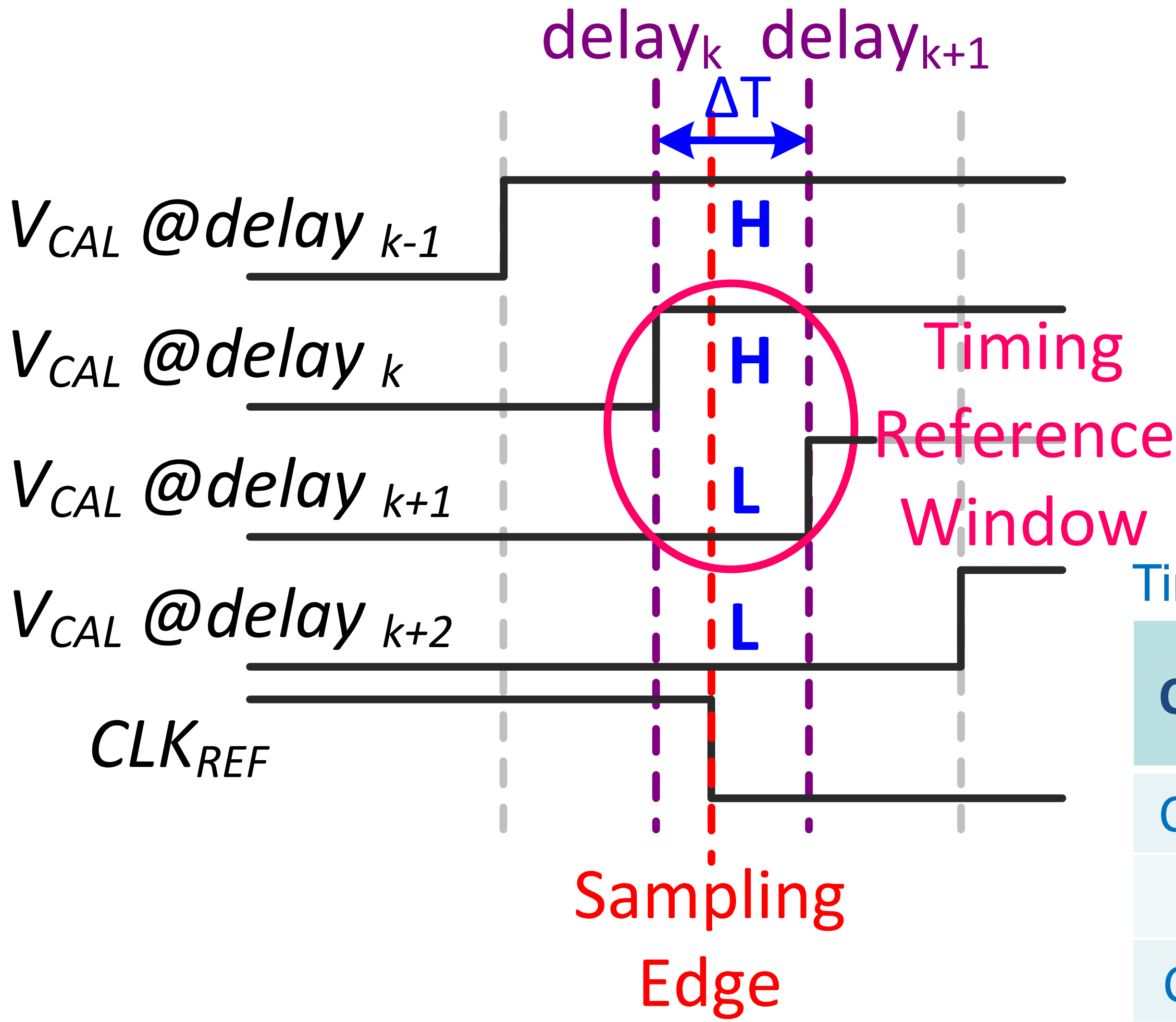
Embedded TDC for CLK_{REF}



Embedded TDC for CLK_{REF}



Timing Reference Windows

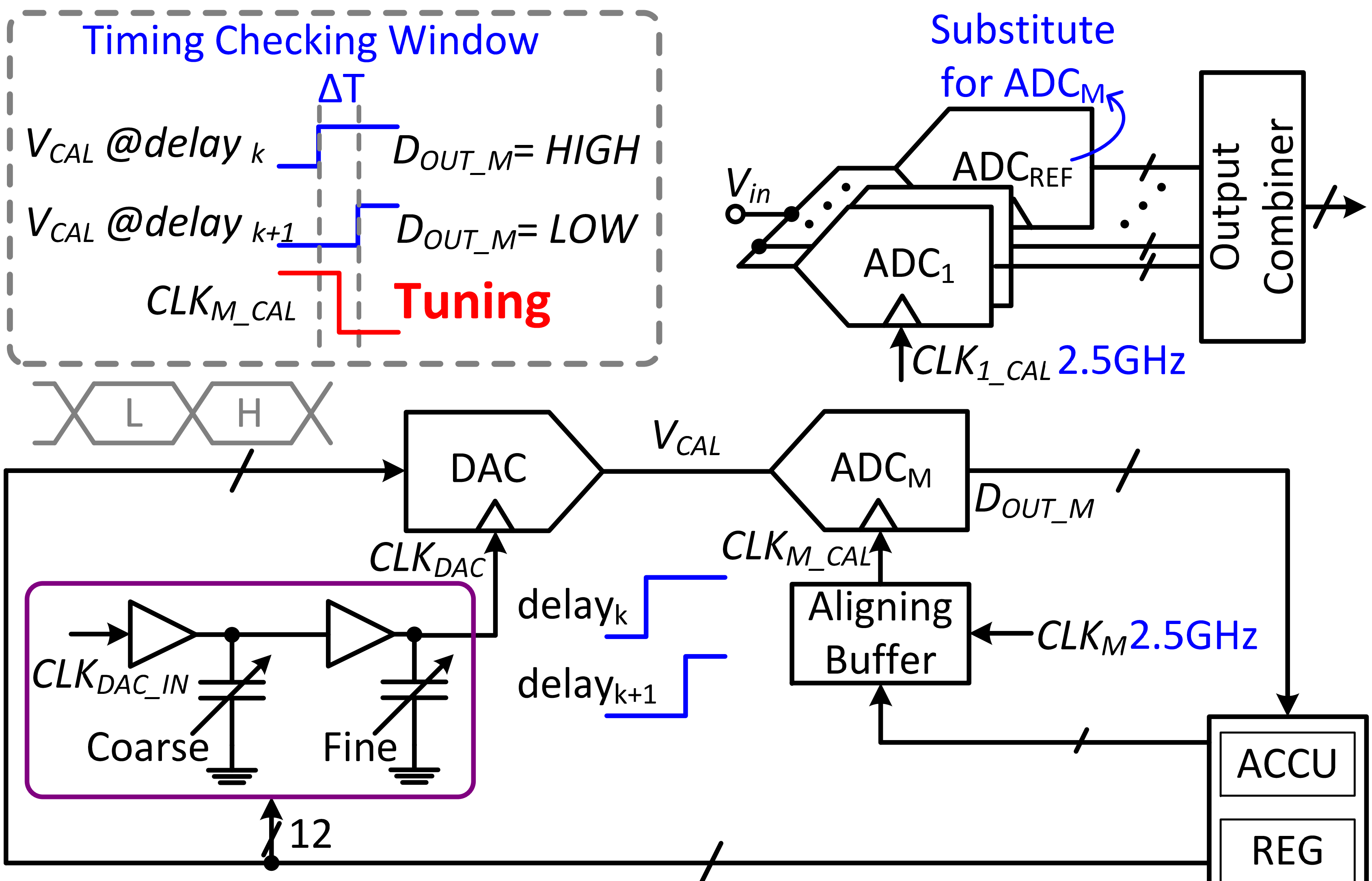


Observe ADC output from H to L & record delay control codes

Timing Reference Windows

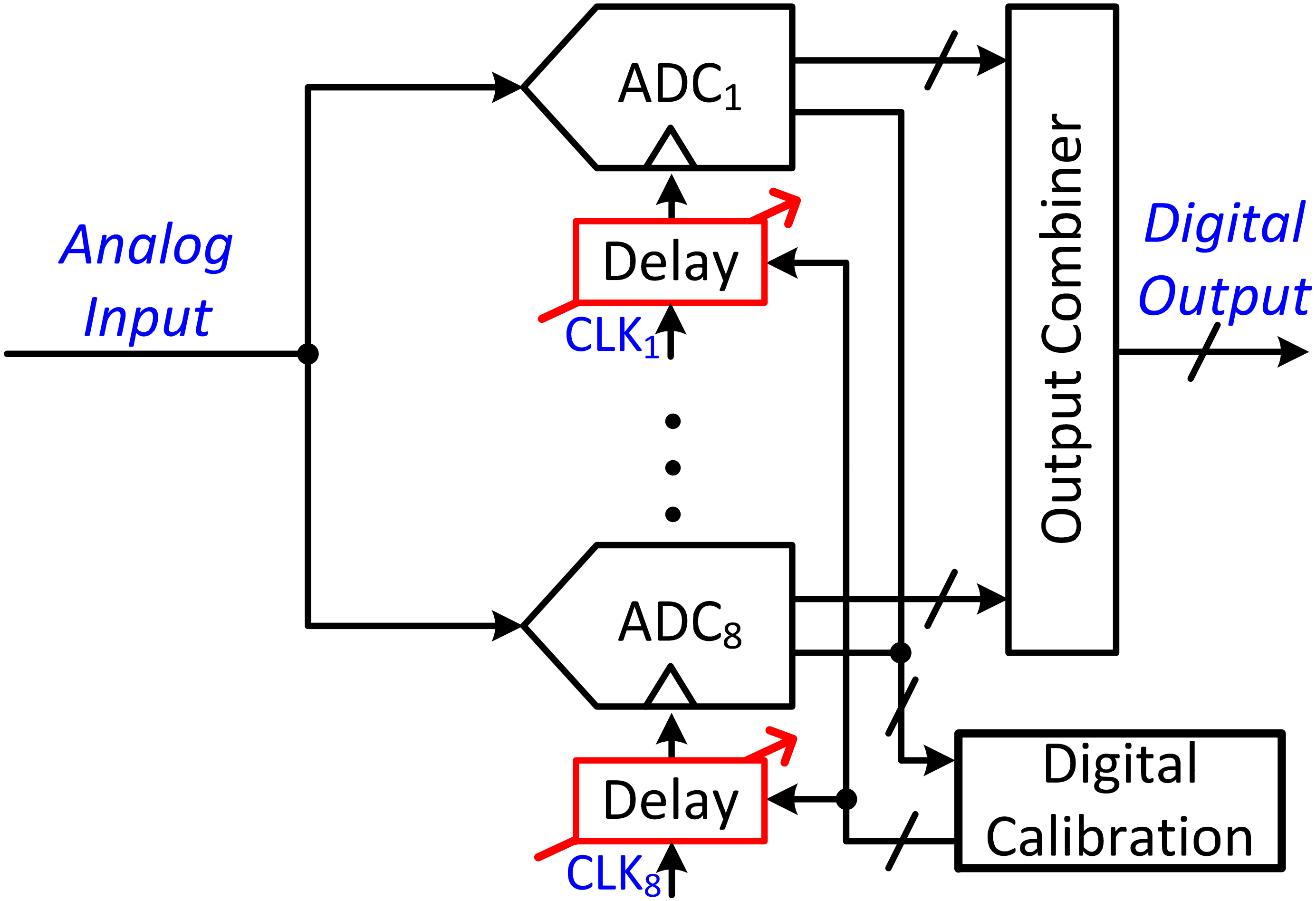
CH #	Code $Delay_k$	Code $Delay_{k+1}$
CH 1	16	17
	• • •	
CH8	967	968

Embedded Time-to-Digital Calibration



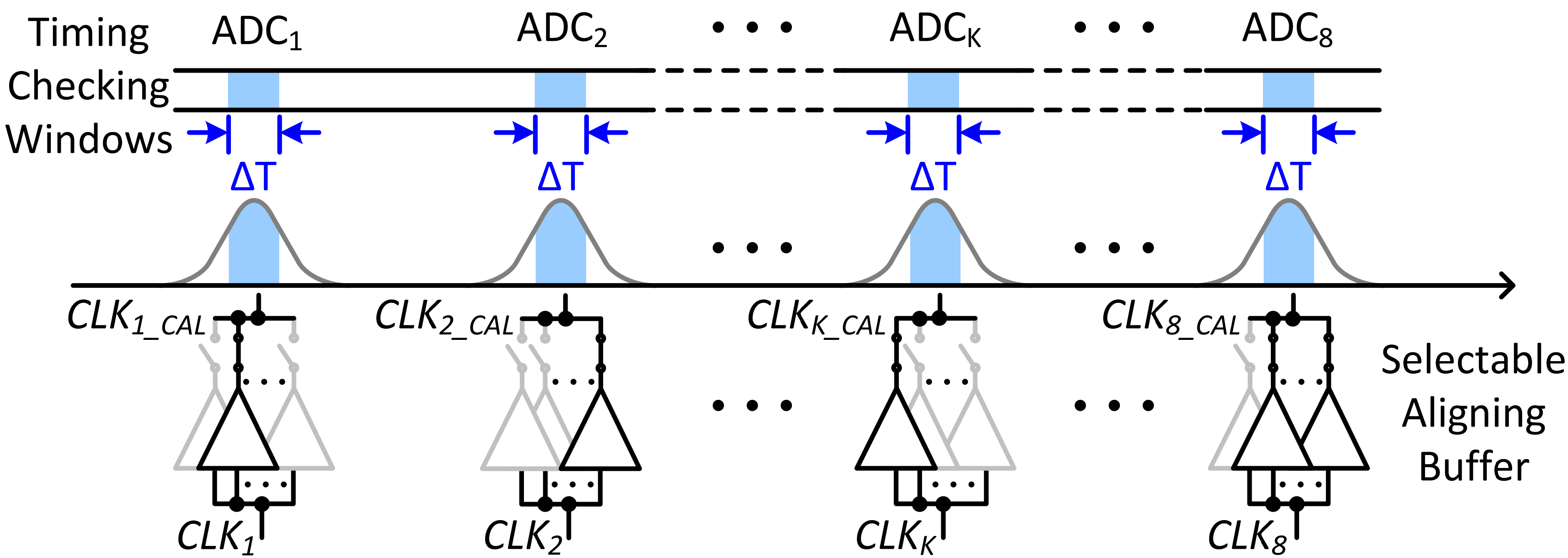
Conventional Tuning Method

- Add delay lines to each channel



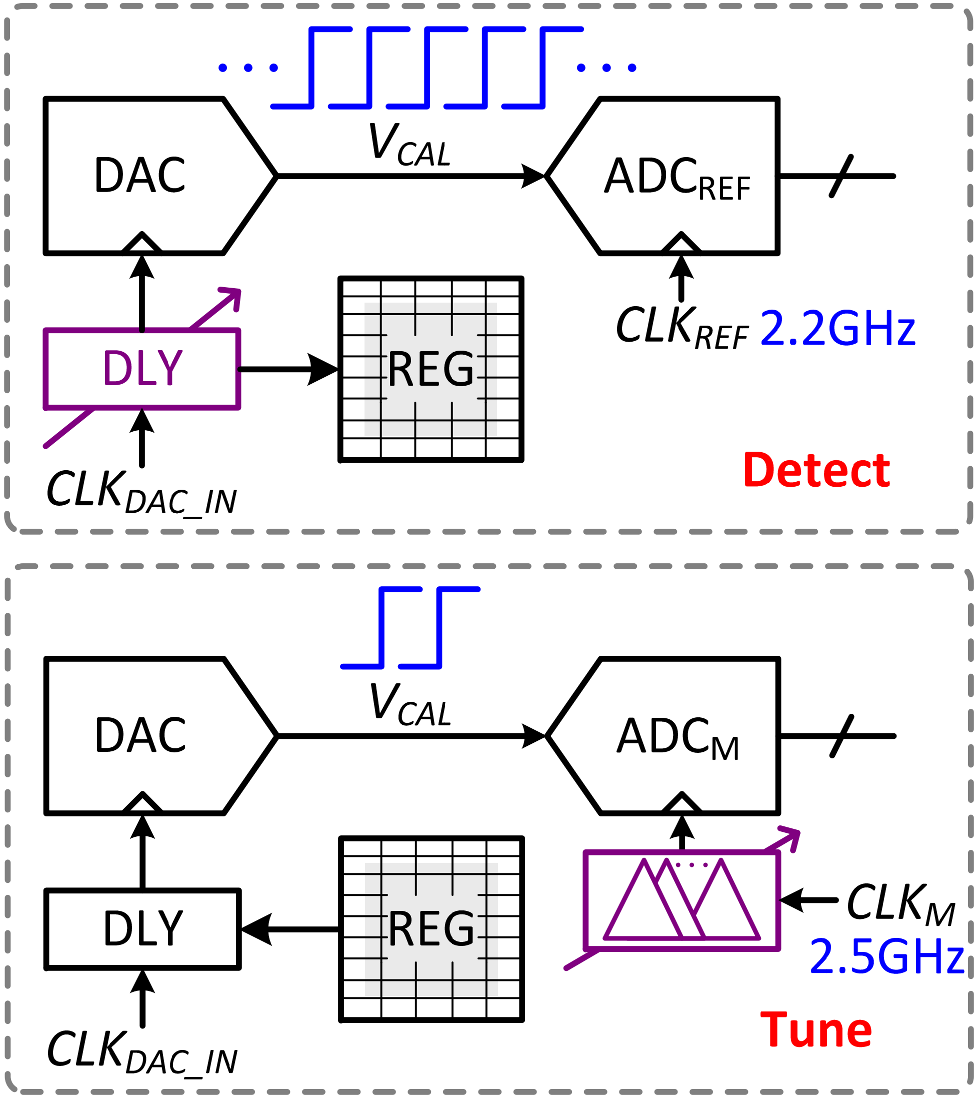
Aligning Buffer

- Choose 6 from 12 clock buffers to form a aligning buffer
- High resolution tuning steps in the time domain



Timing Skew Calibration

- Use ADC as TDC to detect its own sampling edges
- Calibrate ADC_1~ADC_8 with the combinatorial buffers
- No full rate clock (20GHz) required
- Only one delay line
- Low hardware complexity



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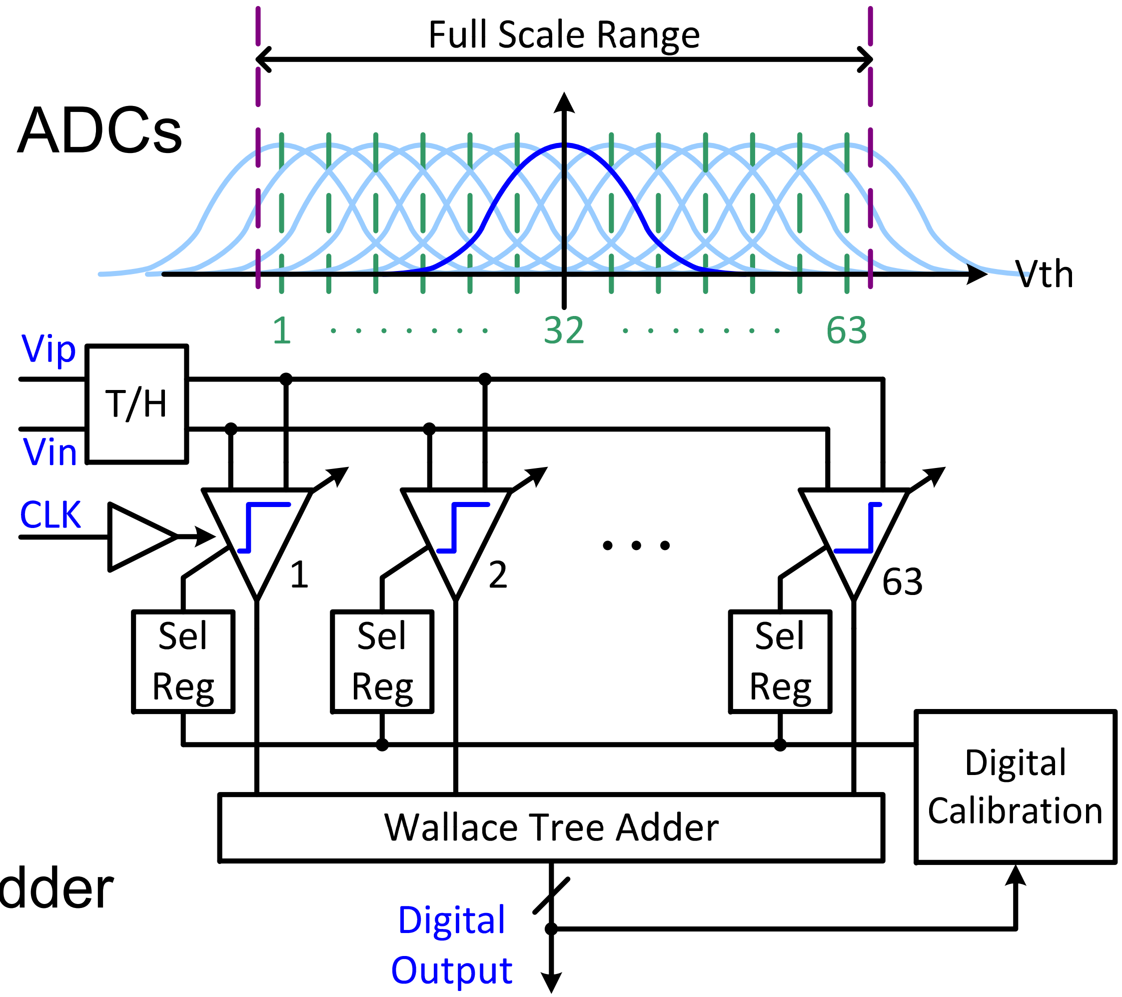
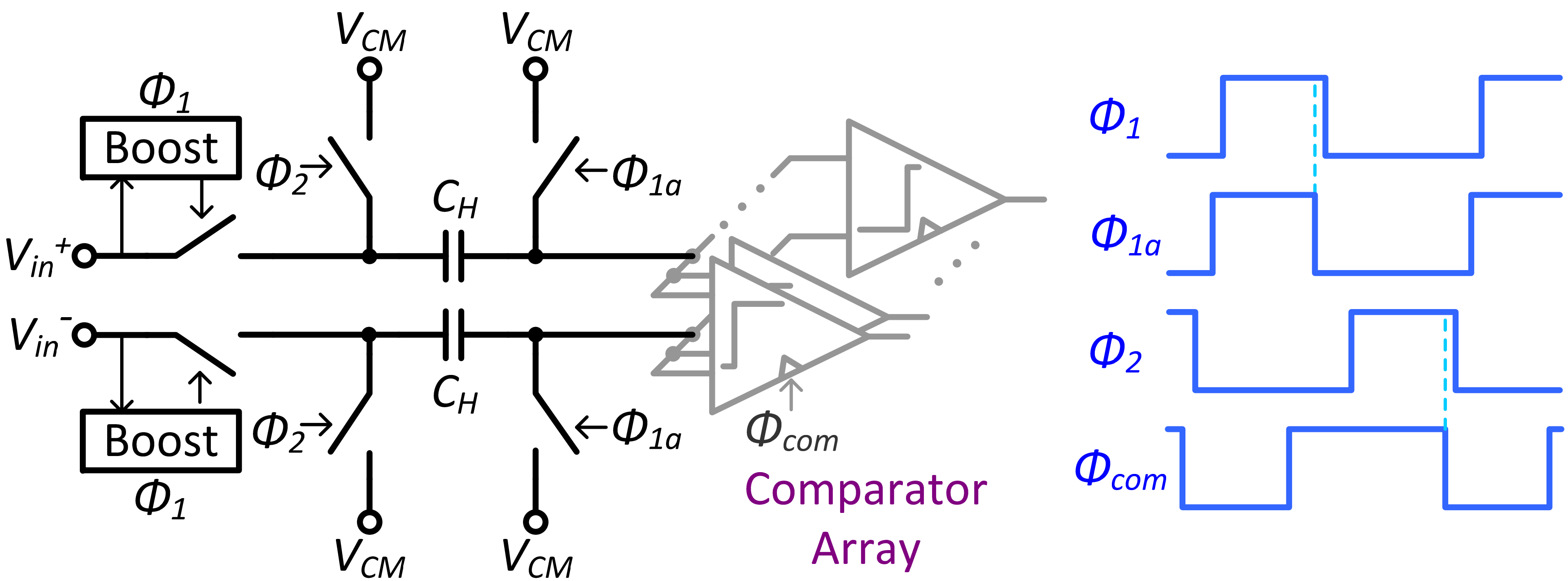
Reference-less Flash ADC

- Reference-less flash ADCs as sub-ADCs
  - ❖ 6-bit @ 2.5GS/s
  - ❖ Minimum sized
  - ❖ Ratioing to create reference levels
  - ❖ Apply calibration
  - ❖ Use Wallace tree adder



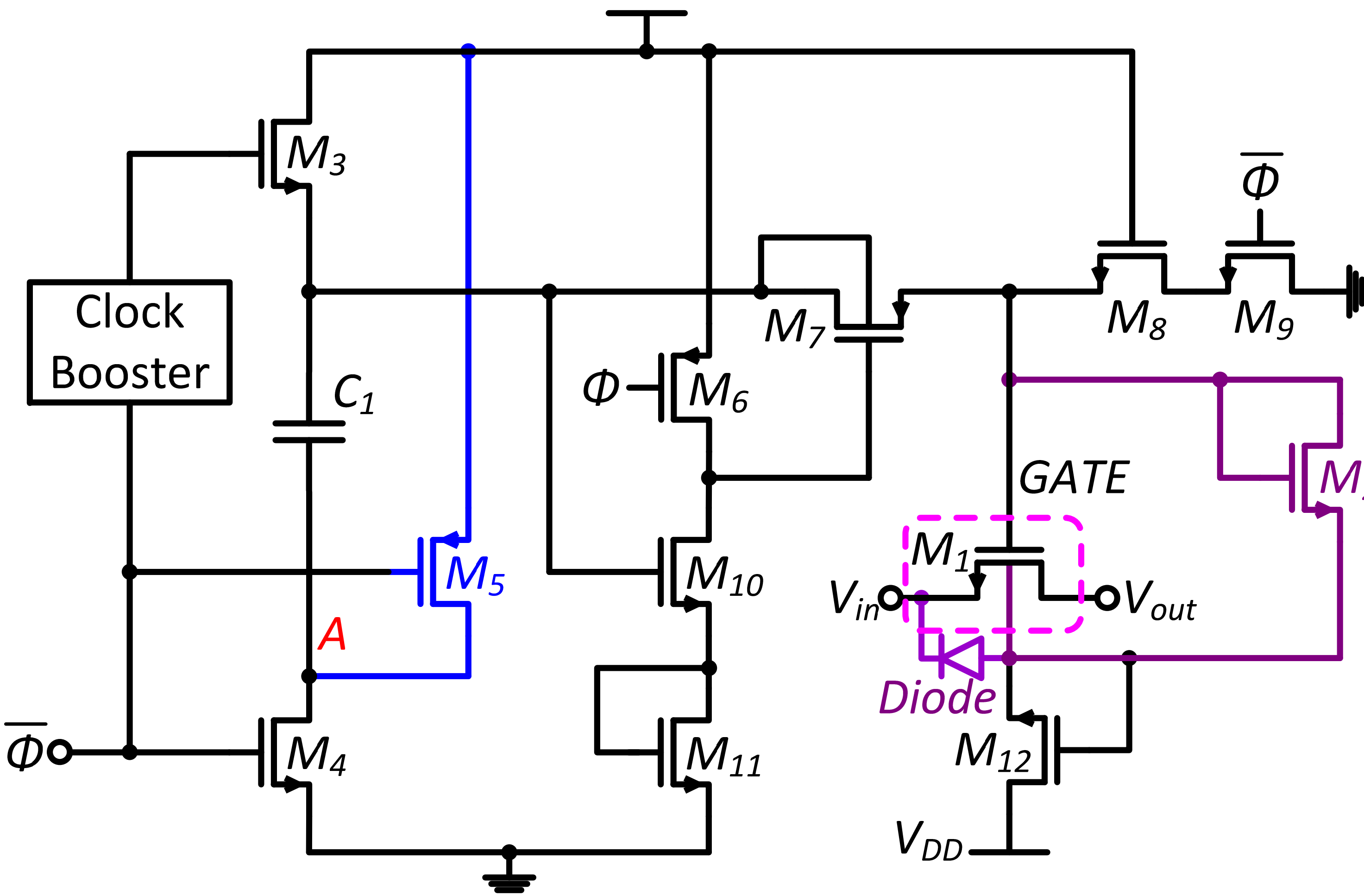
Track and Hold



- Bottom plate sampling with complementary switches as transmission gates
- Boosted input switches to provide better linearity at high speed

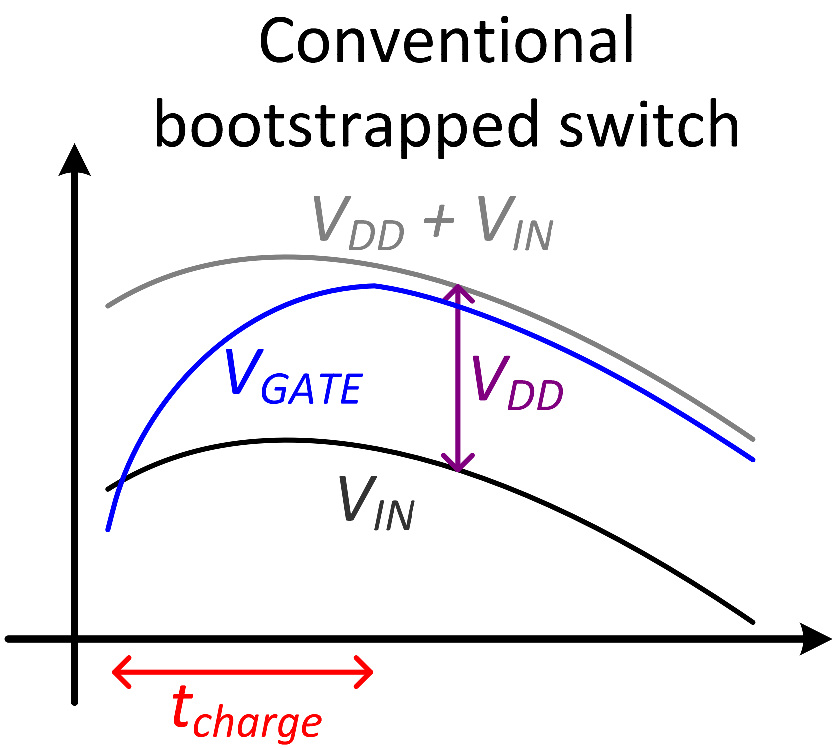
Bootstrapped Input Switch

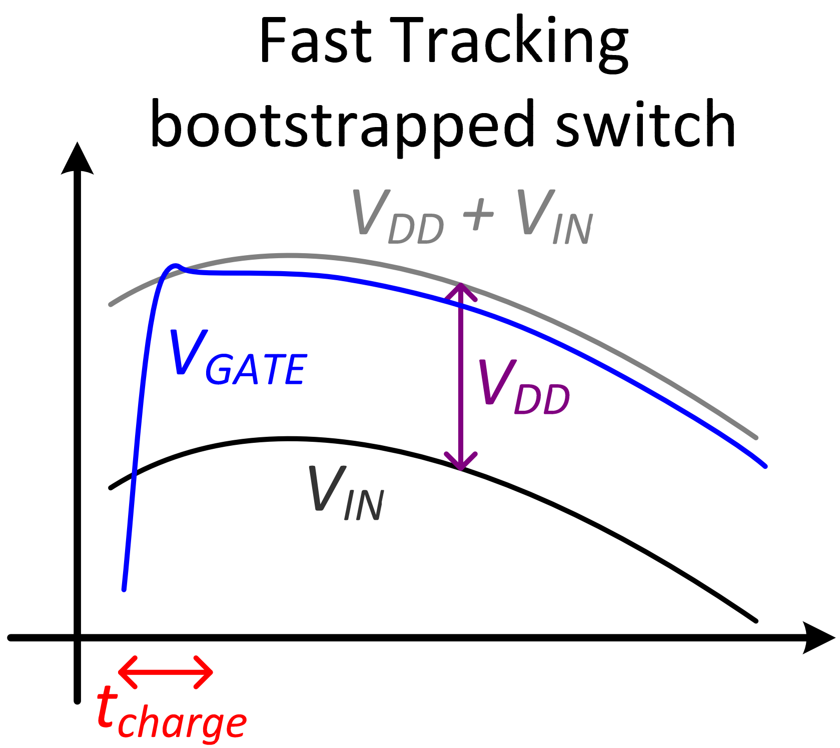
- Fast tracking of input signals to shorten response time



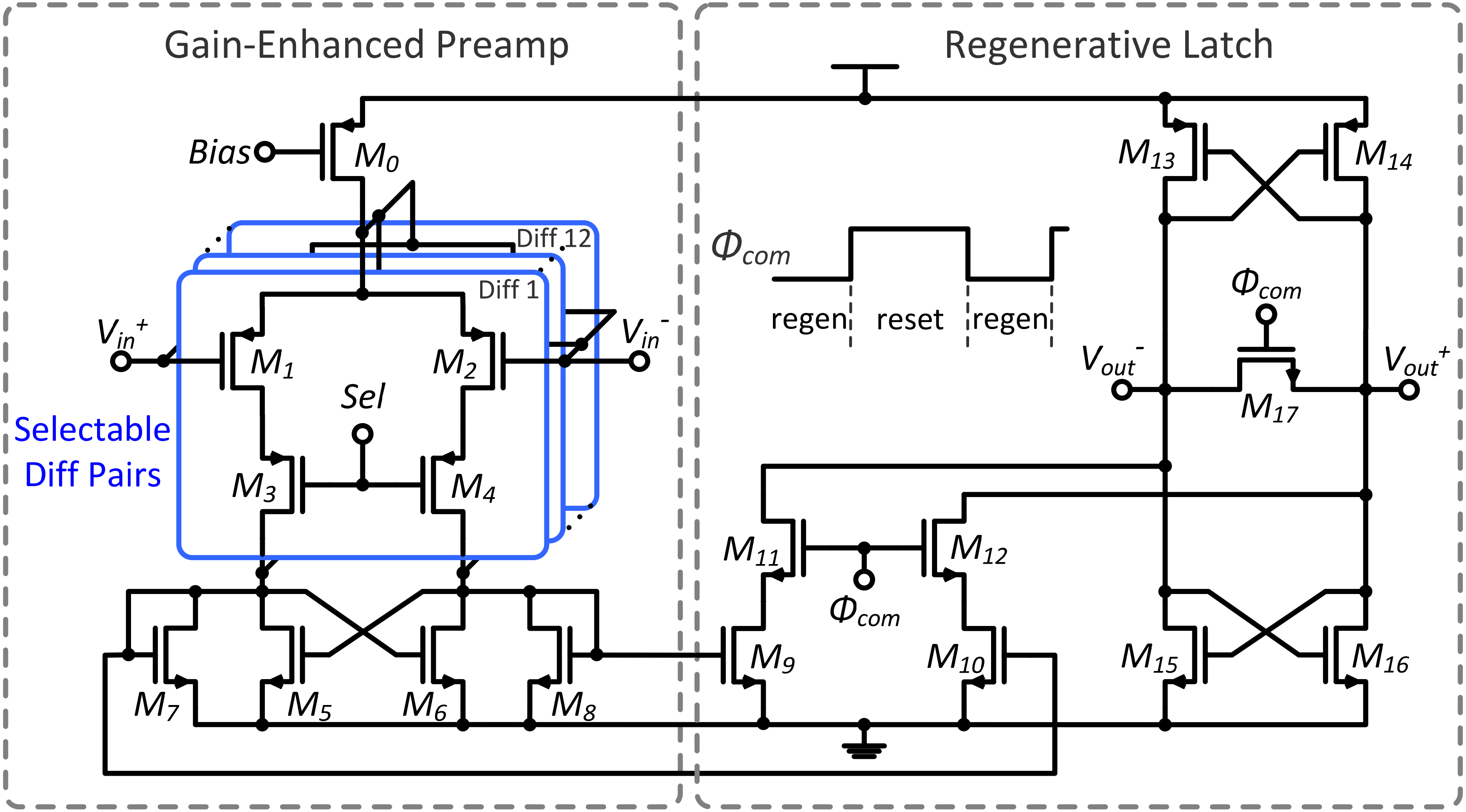
Bootstrapped Input Switch

- Faster compared to the conventional bootstrapped switch
- Charge sharing makes $V_{GATE} < V_{DD}+V_{IN}$
- V_{GS} of input switch is kept lower than V_{DD}



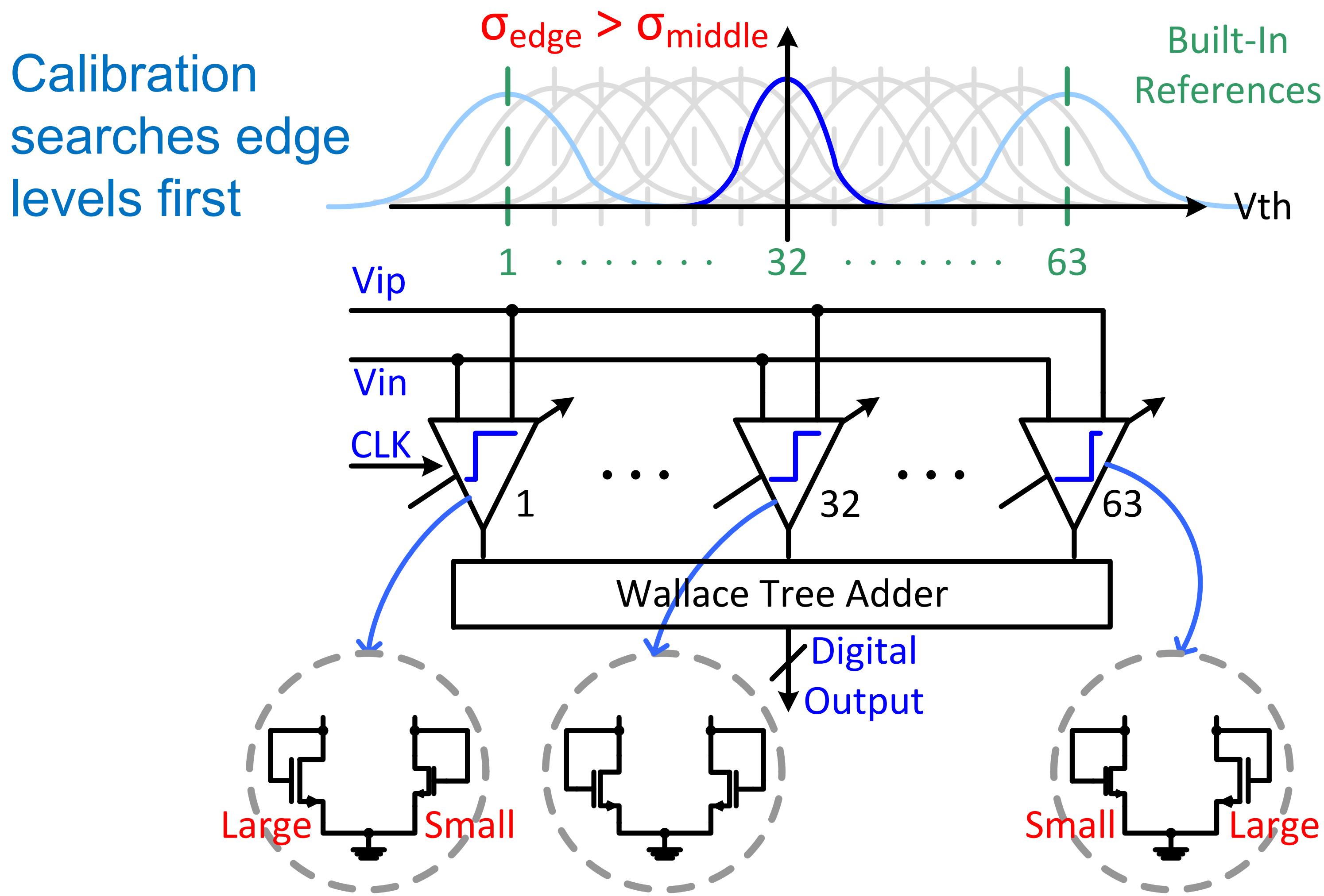


Preamp & Comparator

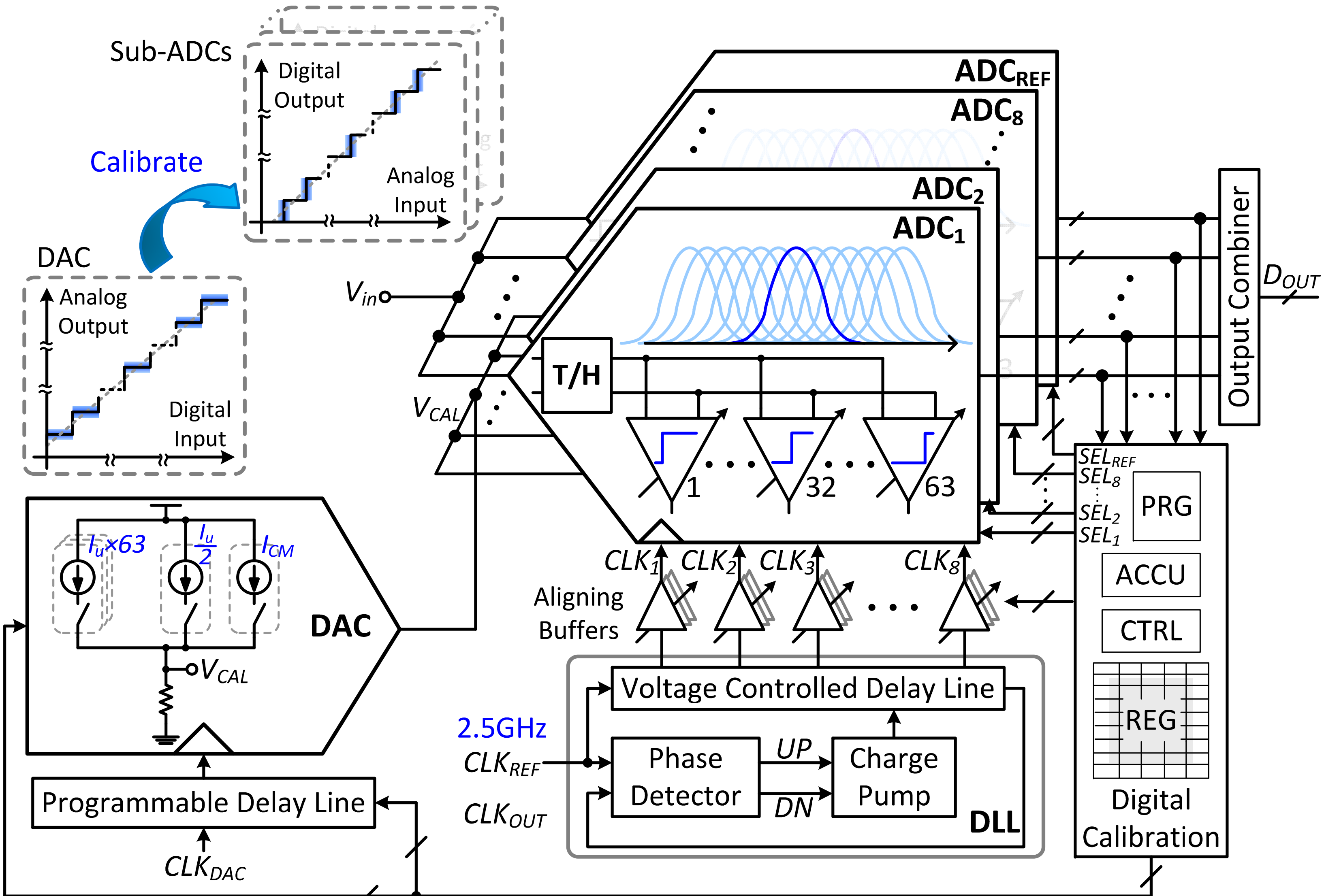


Adder as Encoder

- Comparator can be reassigned arbitrarily with adder

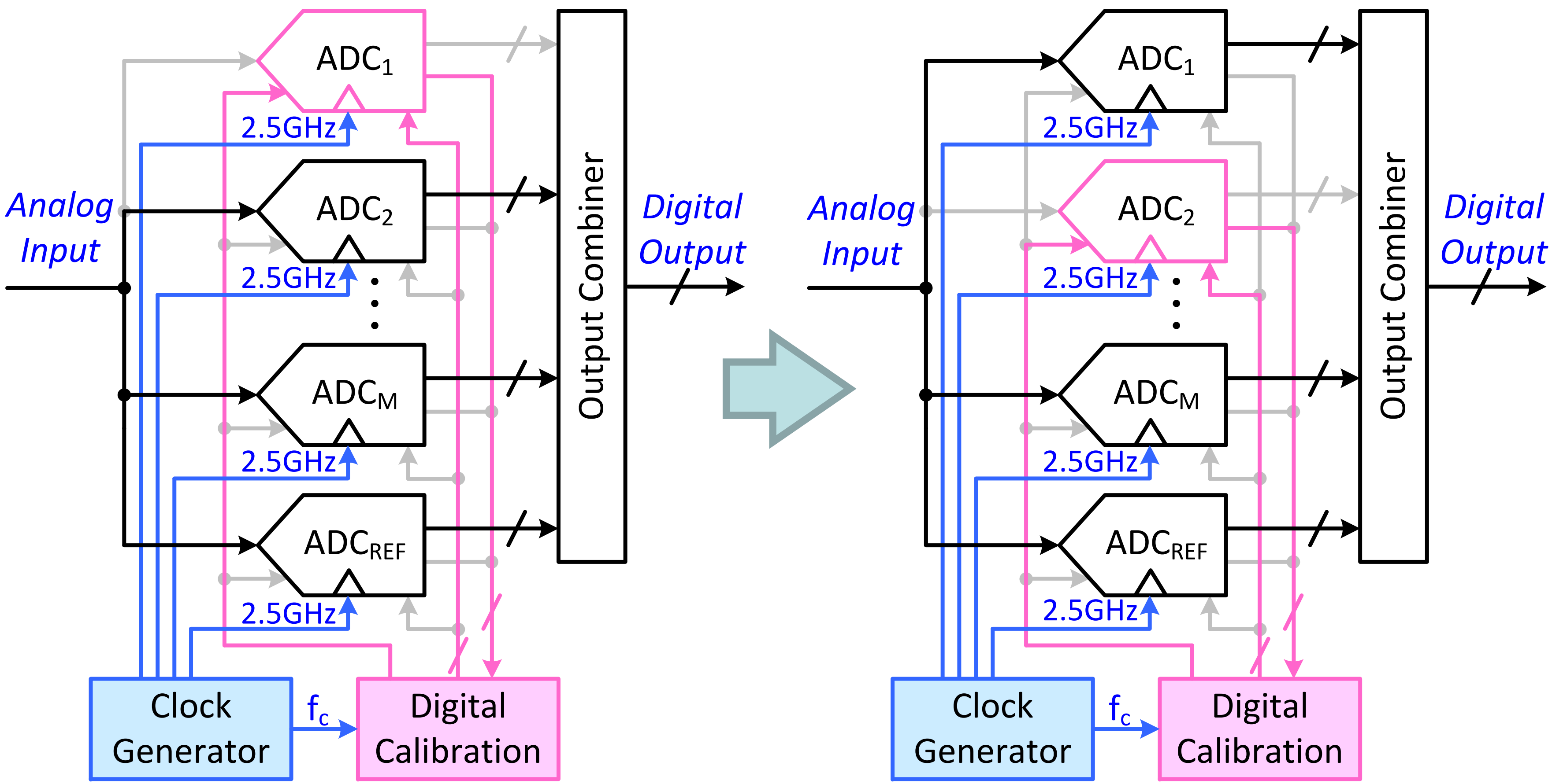


Overall Architecture

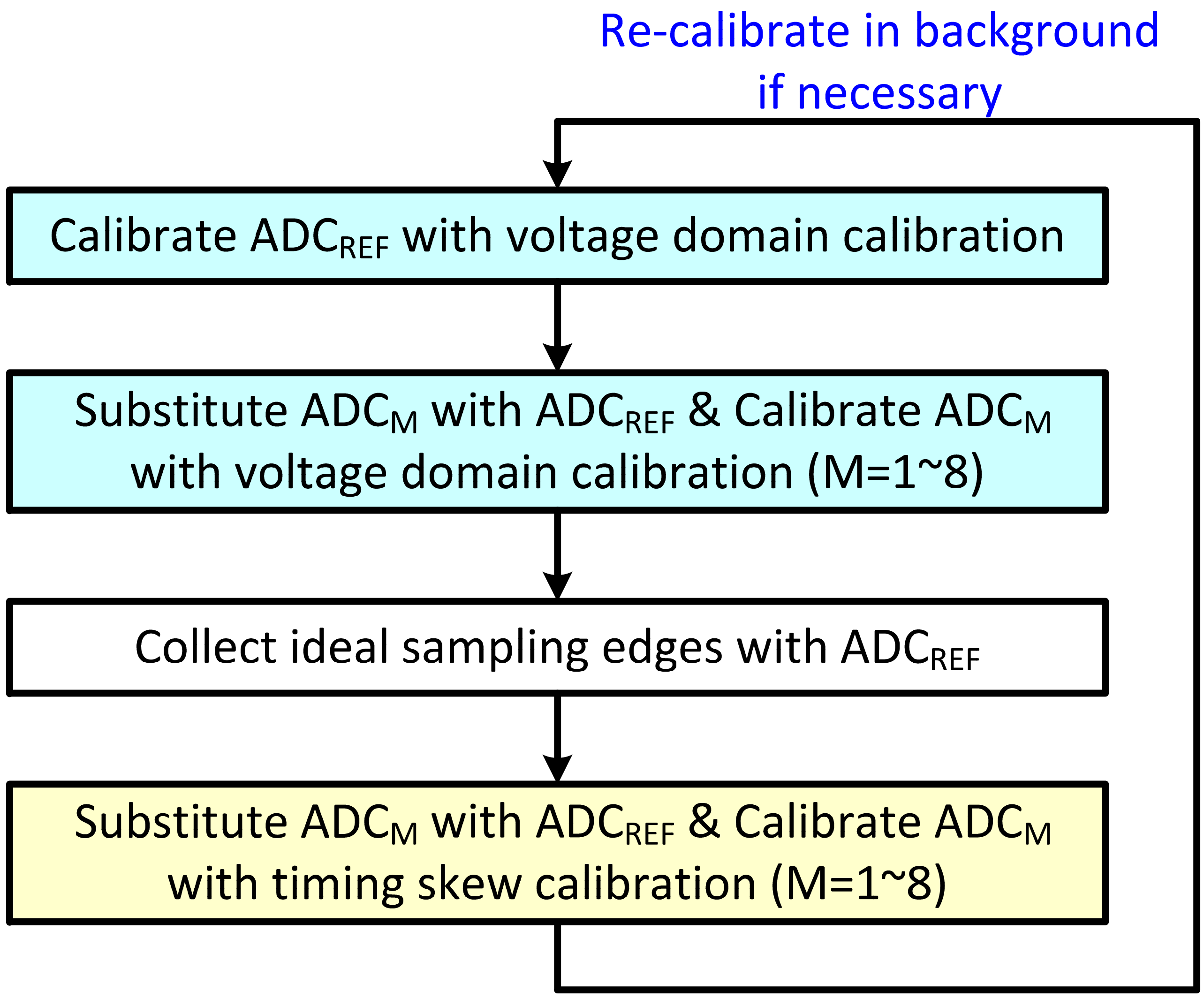


Background Calibration for TI-ADC

- Use ADC_{REF} to periodically substitute for channels that require calibration next



Overall Calibration Sequence

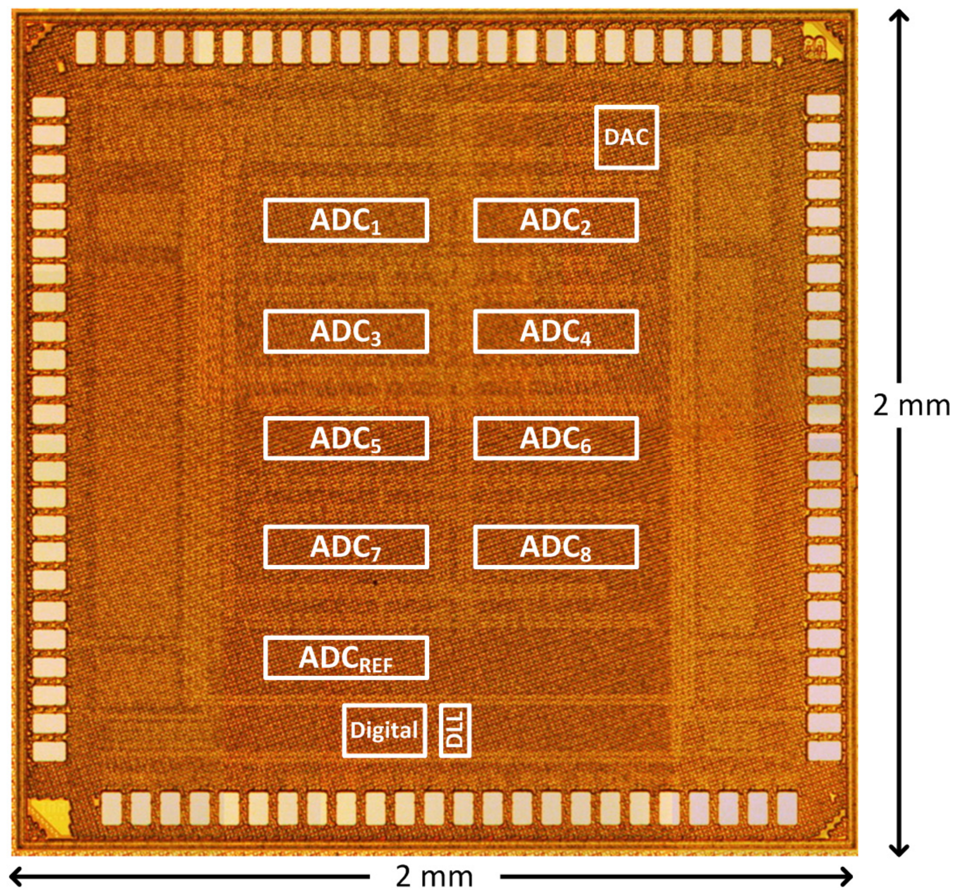


Outline

- Motivation
- Calibration Algorithms
  - Gain and Offset Calibration
  - Embedded Time-to-Digital Calibration
- Circuit Implantation
- Measurement Results
- Conclusions

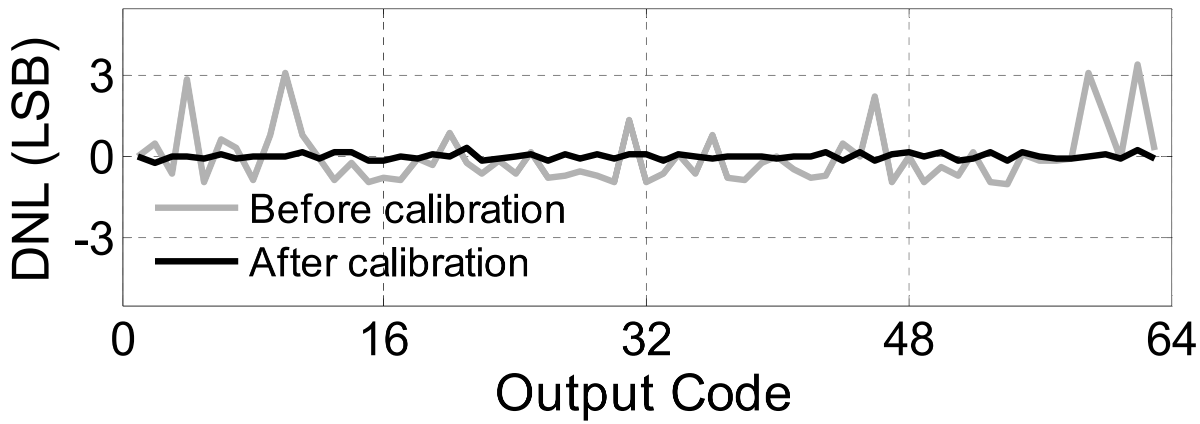
Chip Micrograph

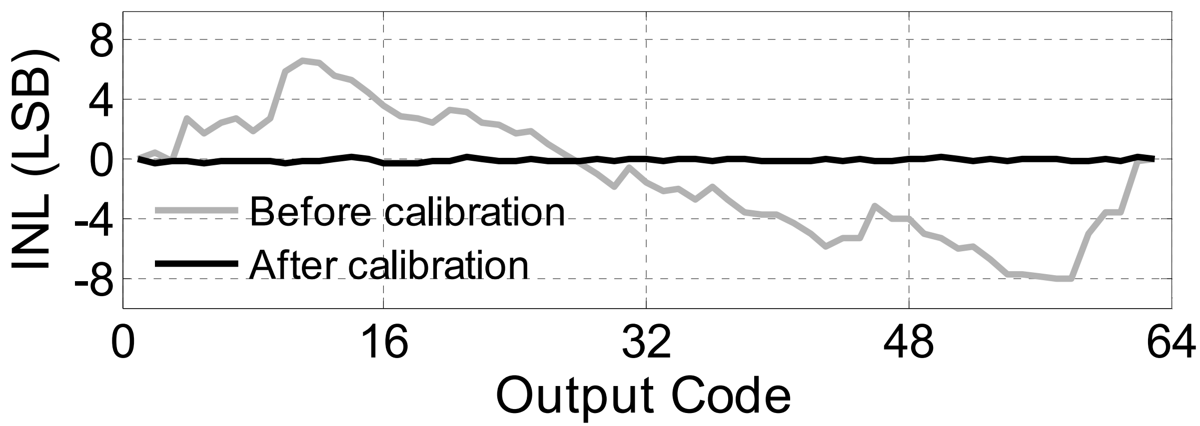
- Implemented in IBM 32nm CMOS SOI process
- Active area < 0.25 mm^2



Measurement Results

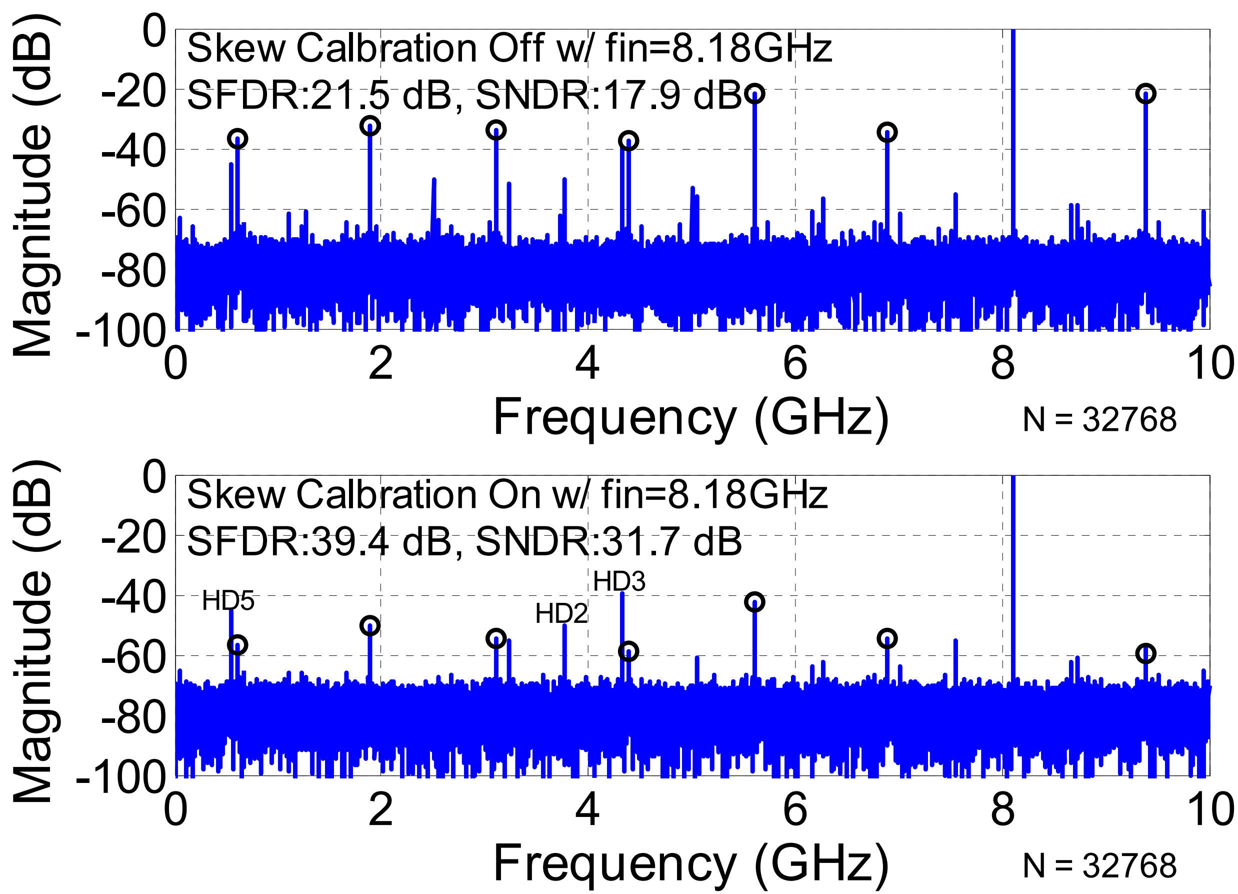
- Static performance
  - DNL: +0.47 /-0.42 LSB, INL: +0.42/-0.38 LSB





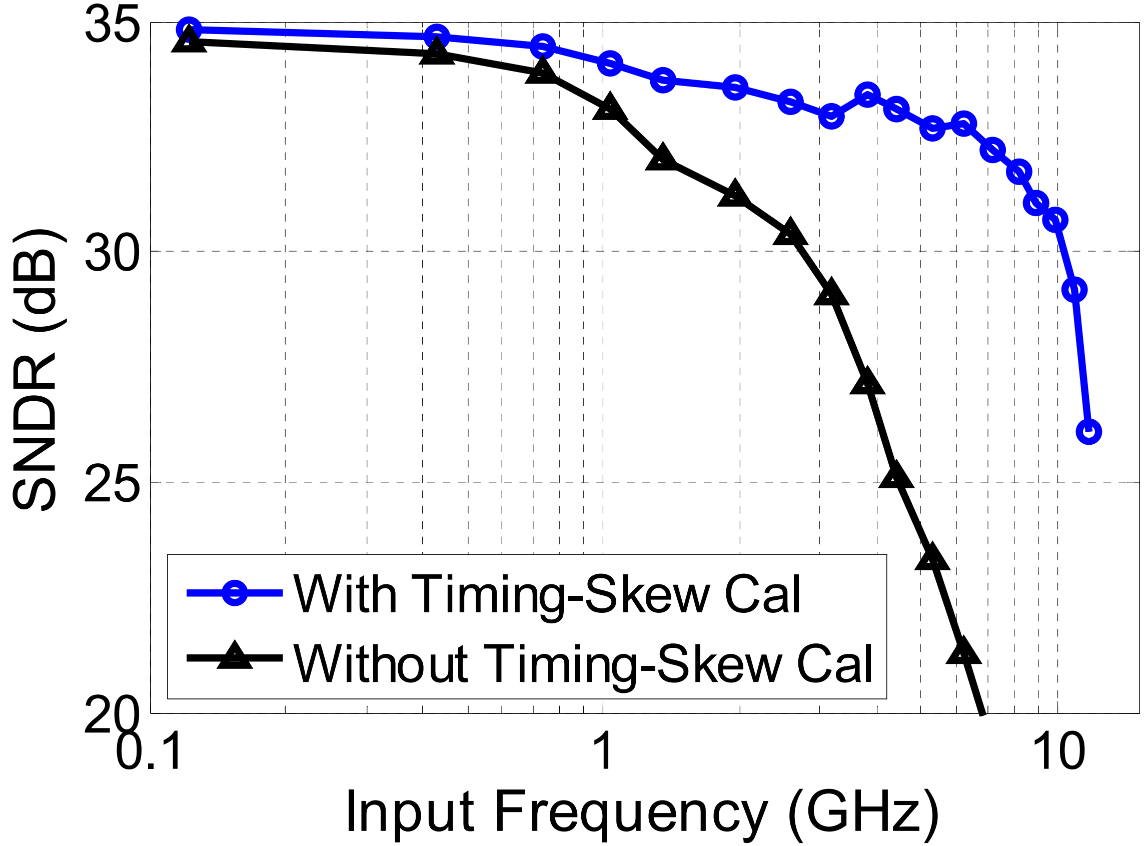
Measurement Results

- Dynamic performance
  - ❖ Largest timing spur is reduced by 20dB



Measurement Results

- Dynamic performance vs. input frequency @ 20GS/s

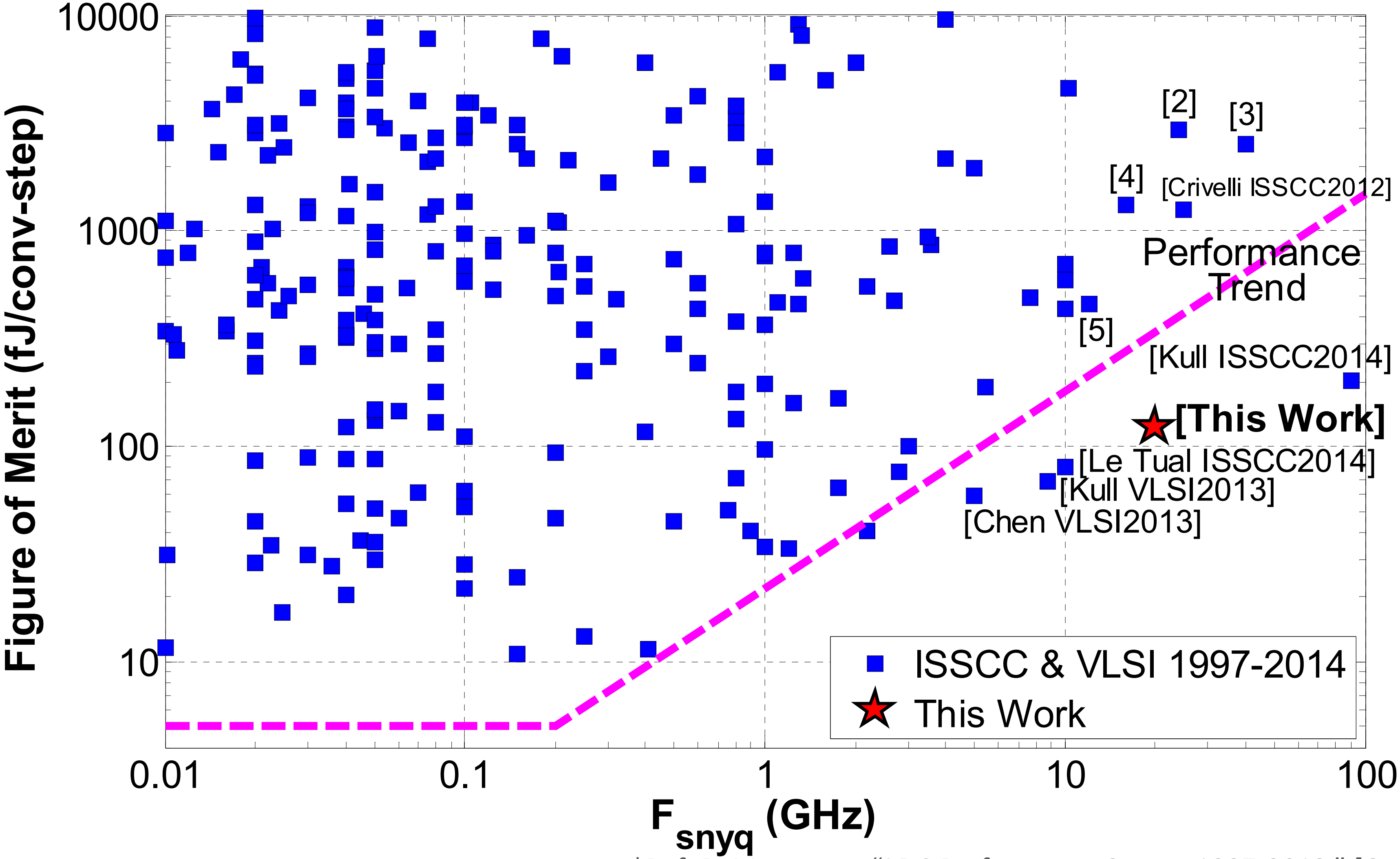


Performance Summary

Technology	32nm CMOS SOI
Supply Voltage	0.9 V
Sampling Rate	20 GS/s
Resolution	6 bits
SFDR @ $f_{Nyquist}$	38.1 dB
SNDR @ $f_{Nyquist}$	30.7 dB
Power Consumption	69.5 mW (Calibration Off) 80.4 mW (Calibration On)
Active Area	0.25 mm^2
FoM @ $f_{Nyquist}$	124 fJ/conv-step

$$*\,FoM = \frac{Power}{2^{ENOB} \times f_{sample}}$$

Performance Comparison



*Ref: B. Murmann, "ADC Performance Survey 1997-2013," [Online]. Available: http://www.stanford.edu/~murmann/adcsurvey.html

Conclusions

- The 69.5mW 20GS/s 6b time-interleaved ADC
  - ❖ Uses small size transistors in comparators and clock buffers
  - ❖ Without full rate clock of 20GHz
  - ❖ Achieves FoM of 124 fJ/conv-step
- Low-complexity calibration to address random mismatch
  - ❖ Use a low frequency signal to align high frequency data
  - ❖ Exploit process randomness to compensate for mismatch
  - ❖ Reduce inter-channel gain/offset mismatch and comparator offset with voltage domain calibration
  - ❖ Reduce timing skew with embedded time-to-digital calibration

Acknowledgments

- The authors would like to acknowledge the financial support of FCRP C2S2

- The authors would like to thank the following people for discussion
  - ❖ Rick Carley of CMU
  - ❖ Jeff Weldon of CMU
  - ❖ Jeyanandh Paramesh of CMU
  - ❖ Ethan Chen of CMU
  - ❖ Jean-Olivier Plouchart of IBM
  - ❖ Chao-Cheng Lee of Realtek Semiconductor

A 20GHz-BW 6b 10GS/s 32mW Time-Interleaved SAR ADC with Master T&H in 28nm UTBB FDSOI Technology

Stéphane Le Tual[1], Pratap Narayan Singh[2], Christophe Curis[3], Pierre Dautriche[1]

[1]*STMicroelectronics, Crolles, France,*
[2]*STMicroelectronics, Greater Noida, India,*
[3]*STMicroelectronics, Grenoble, France*

life.augmented

Motivations

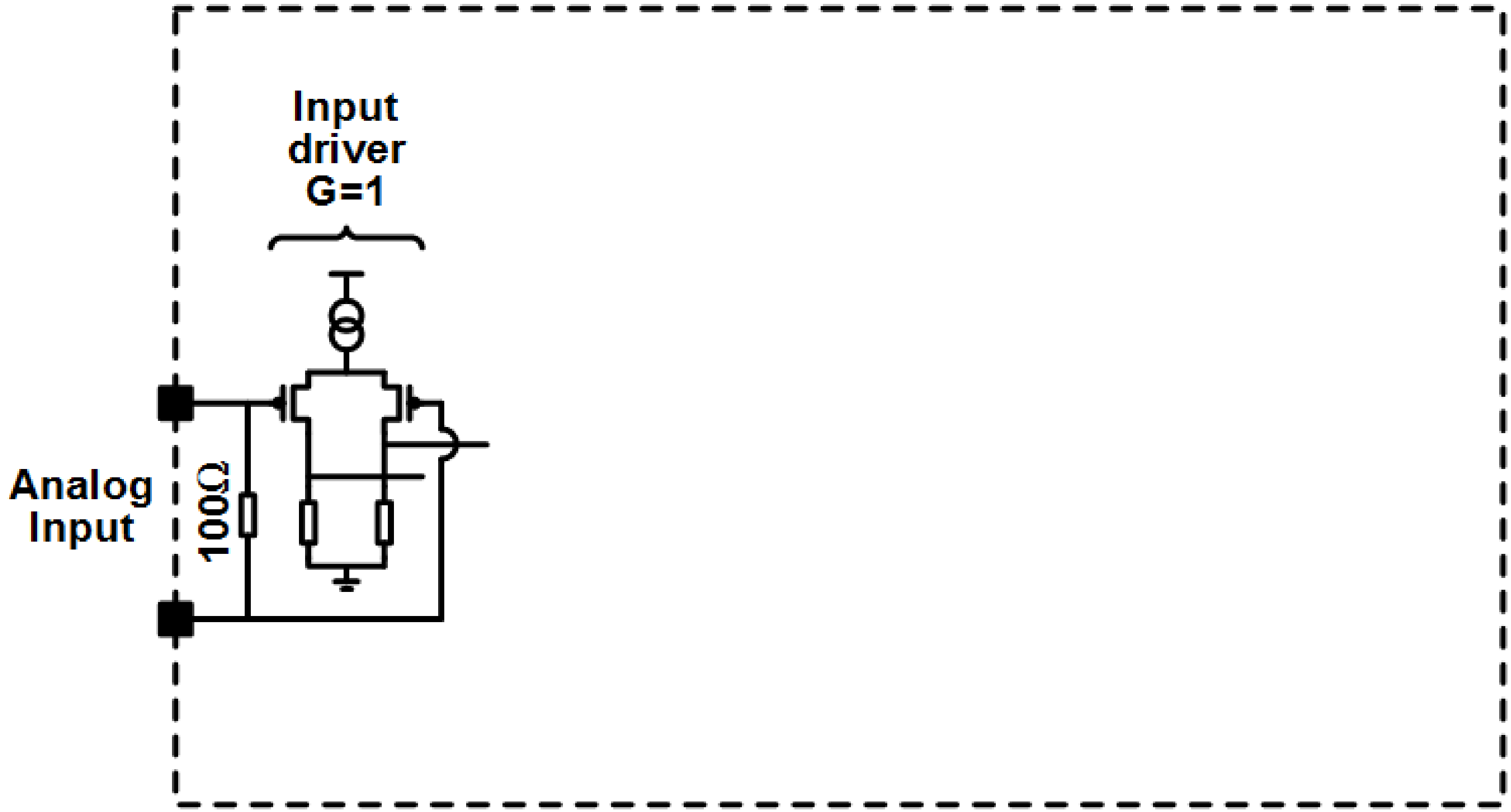
- Basic building block for high-speed serial links receivers
  – To perform digital equalization
  – or demodulation (QPSK, 16QAM)

- 28nm UTBB FDSOI technology demonstration for high-speed mixed-signal application

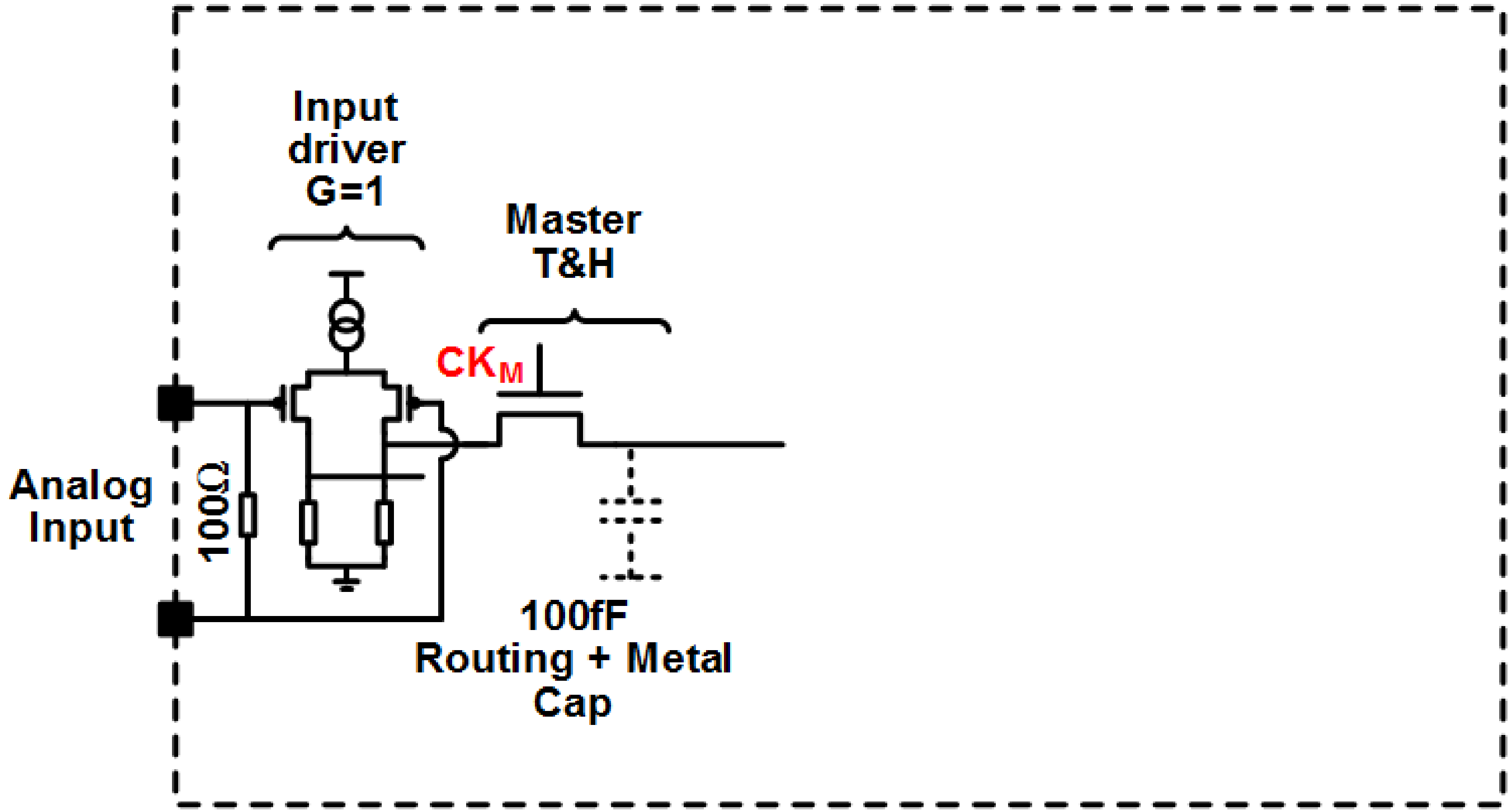
Outline

- Architecture
- Technology
- Design details
- Layout
- Module assembly
- Measurements
- Conclusion

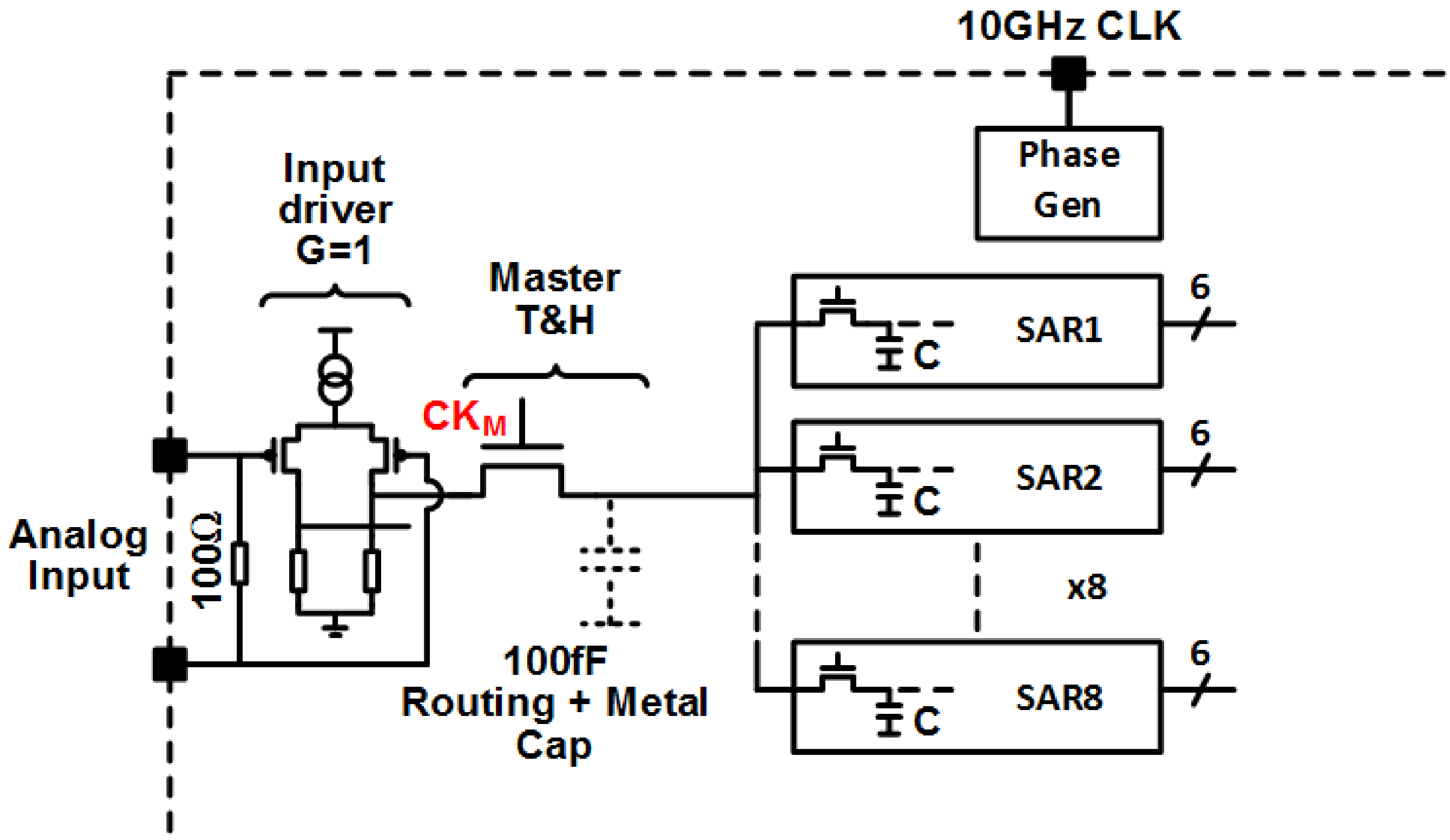
Architecture



Architecture

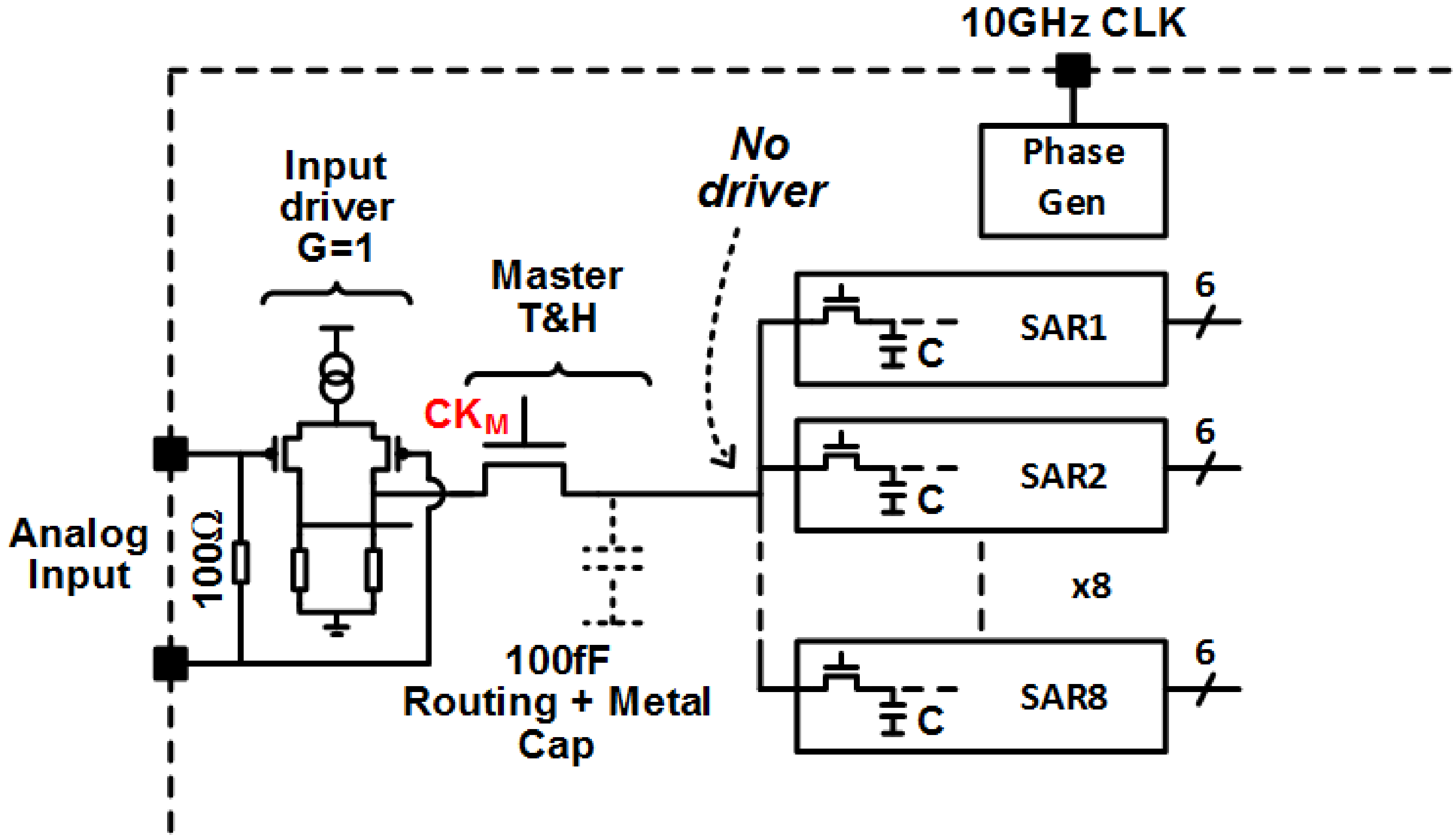


Architecture



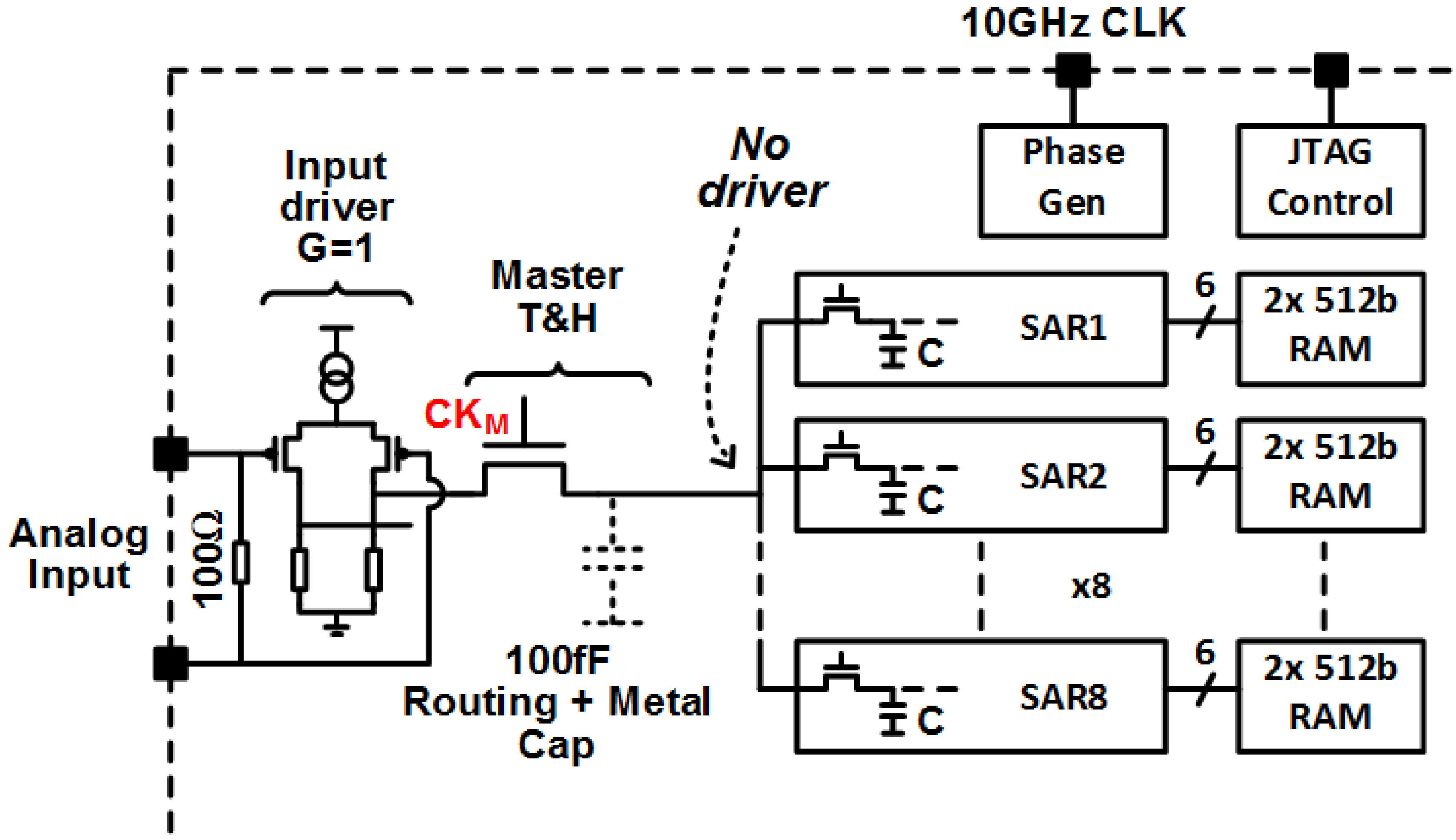
- Master T&H to avoid any skew & bandwidth mismatches

Architecture



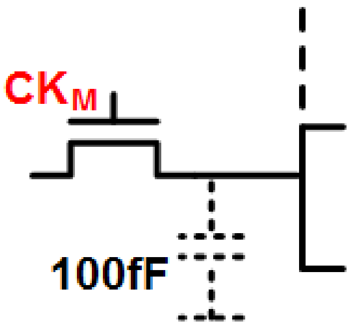
- Master T&H to avoid any skew & bandwidth mismatches

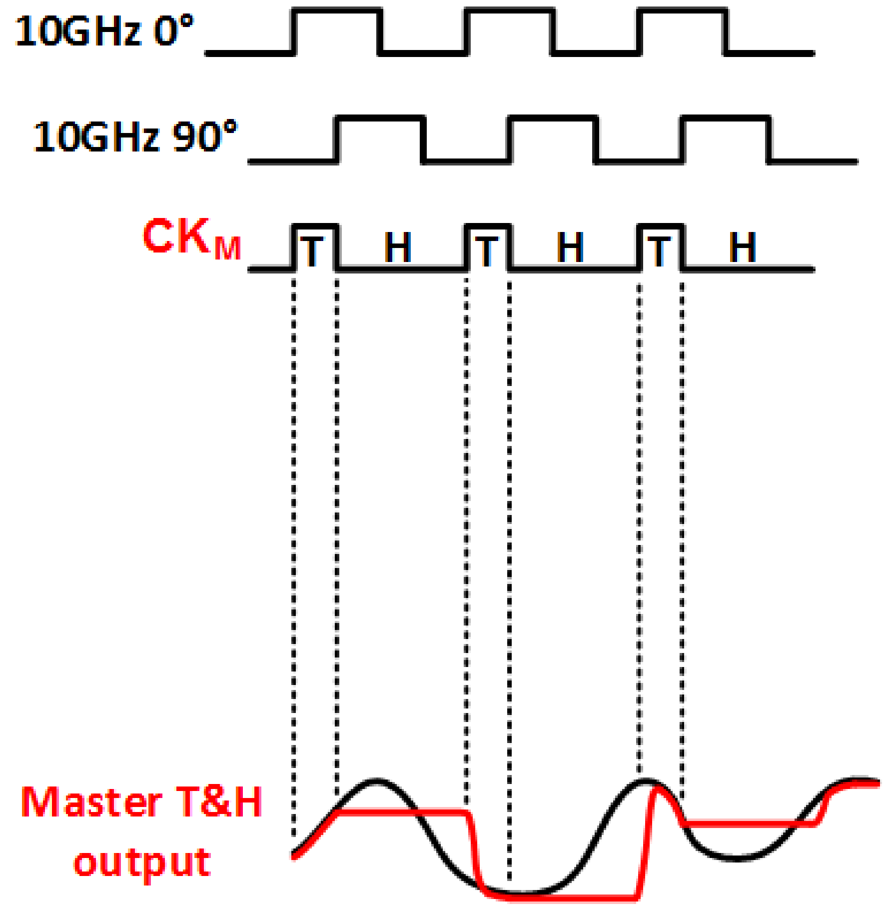
Architecture



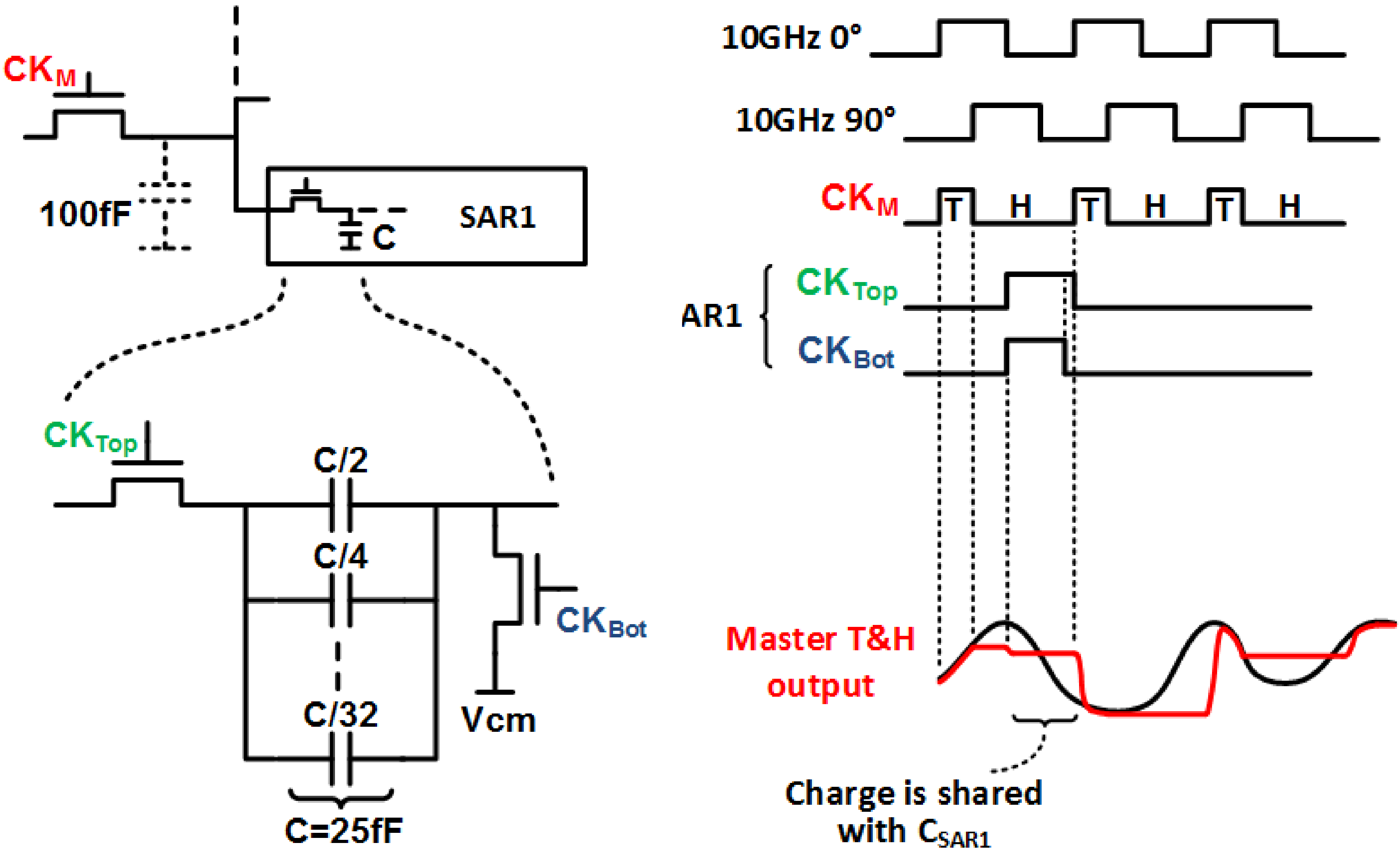
- Master T&H to avoid any skew & bandwidth mismatches

Sample & redistribute timing diagram

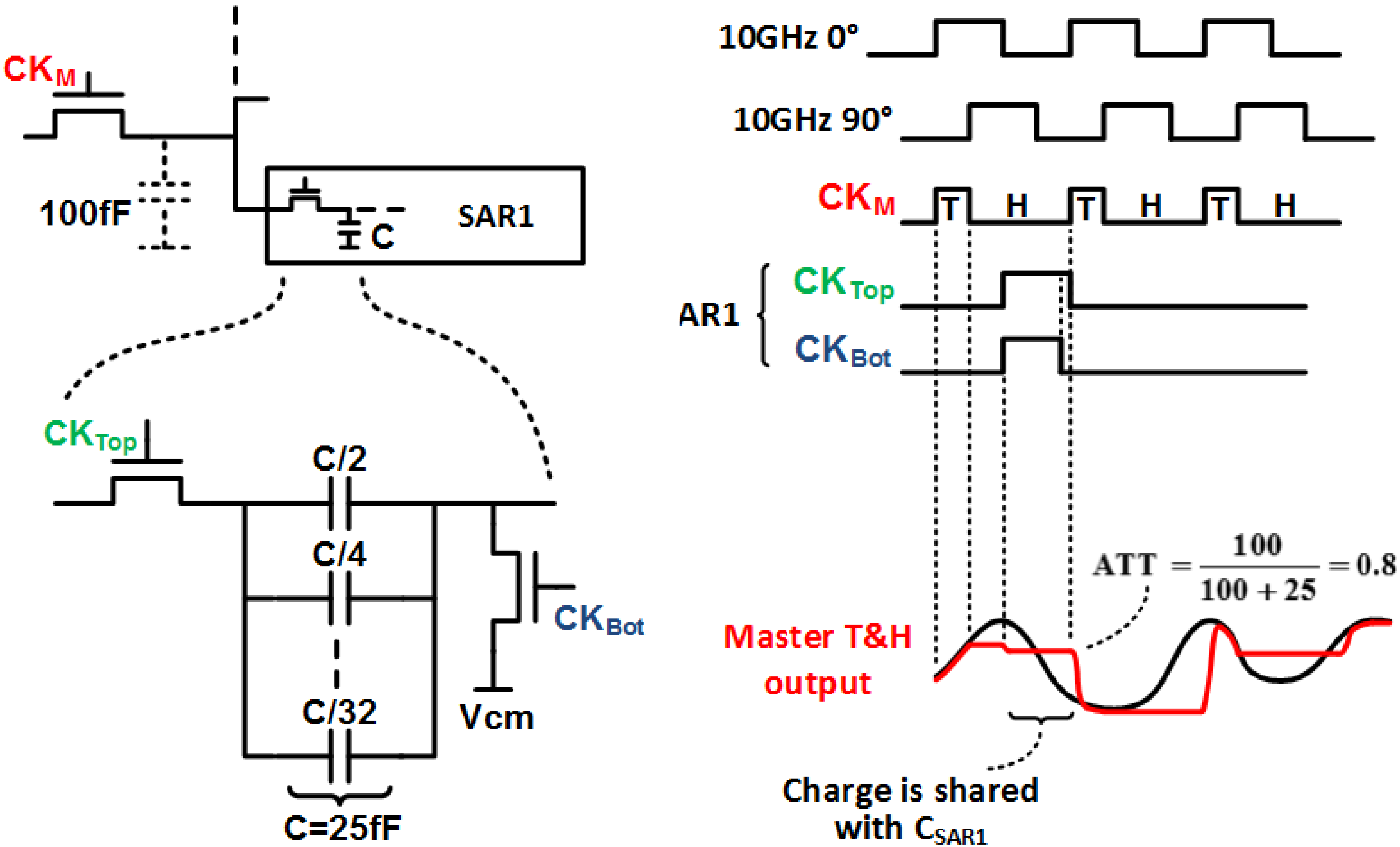




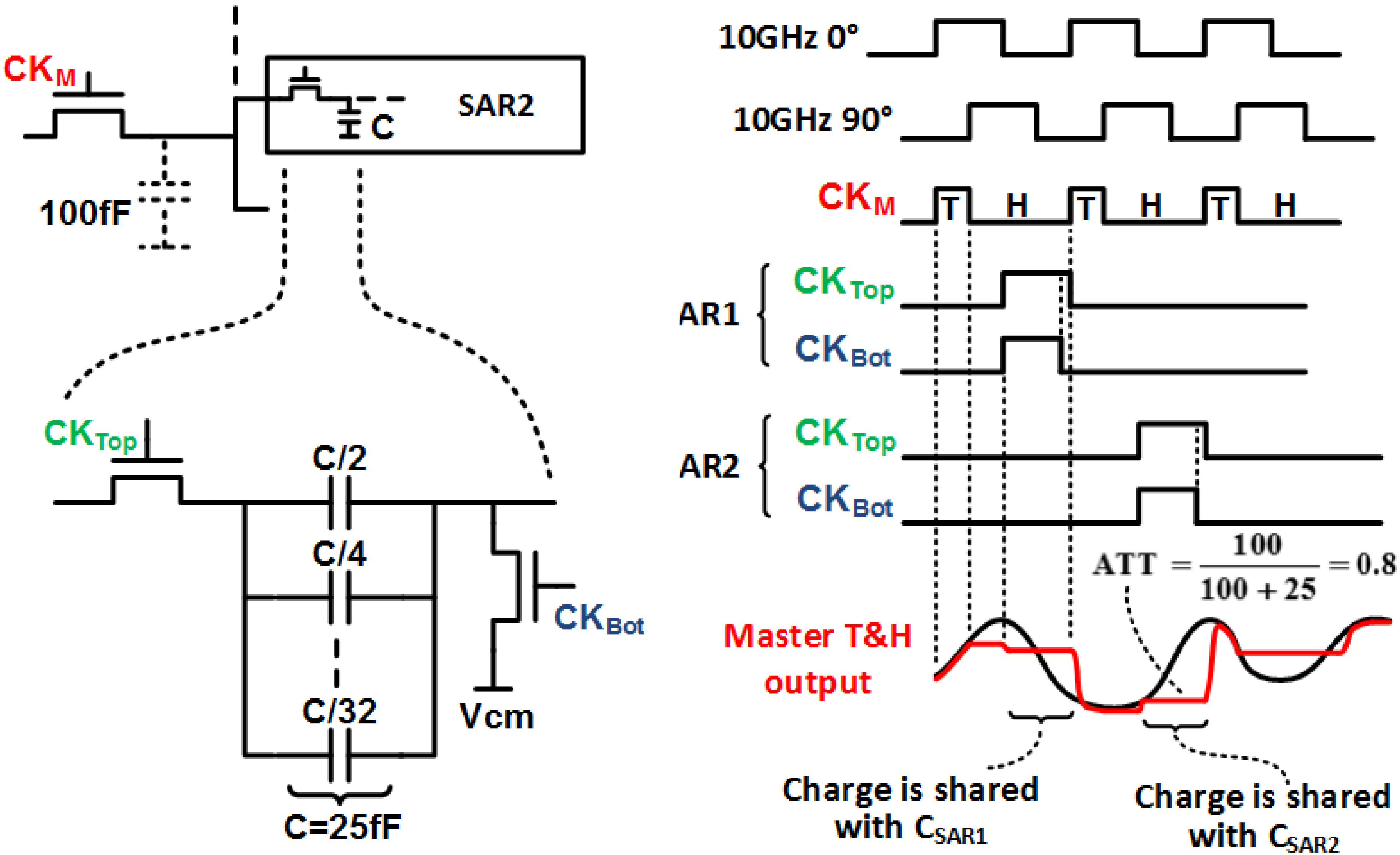
Sample & redistribute timing diagram



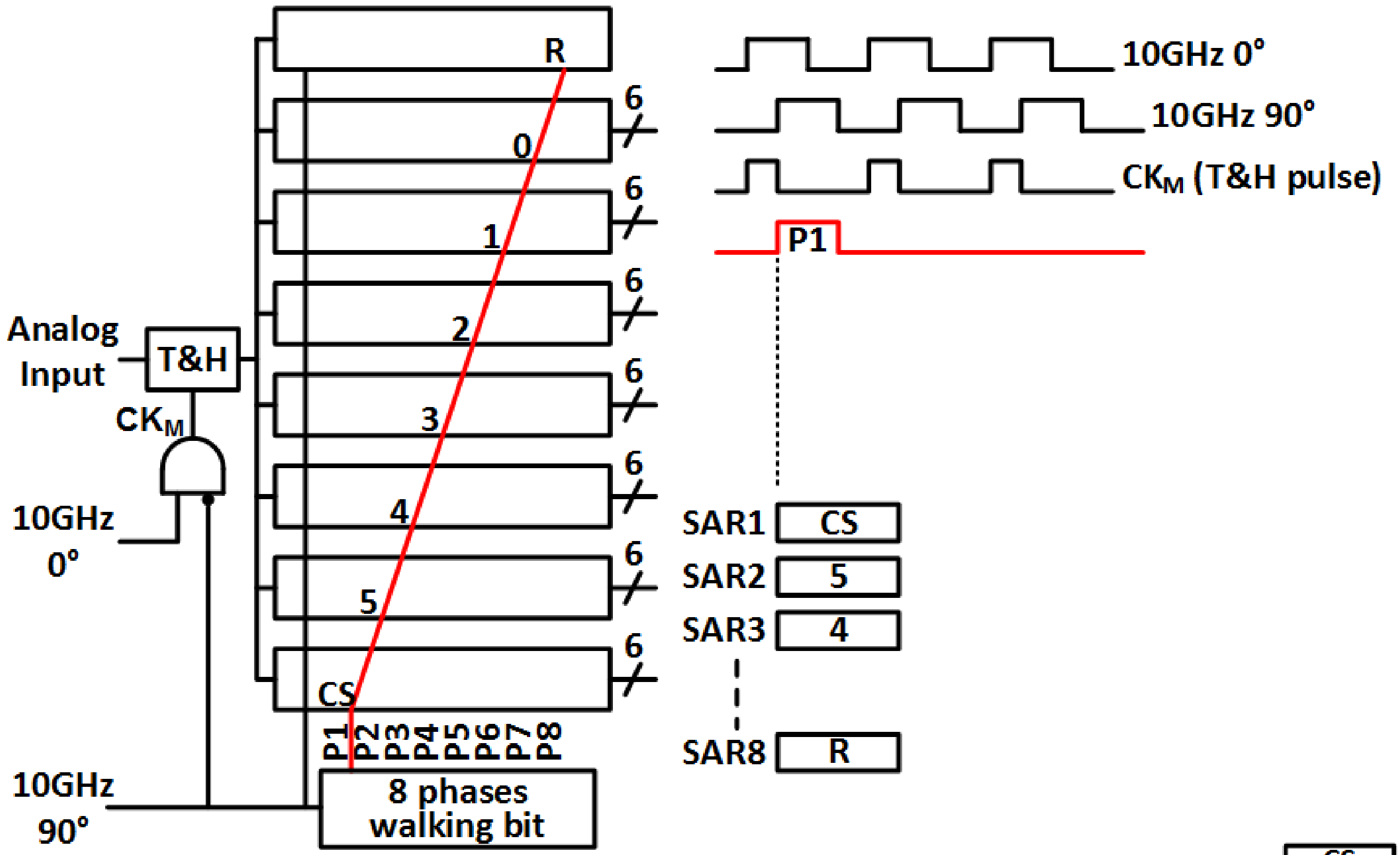
Sample & redistribute timing diagram



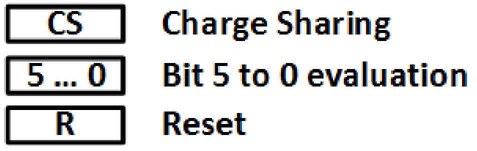
Sample & redistribute timing diagram



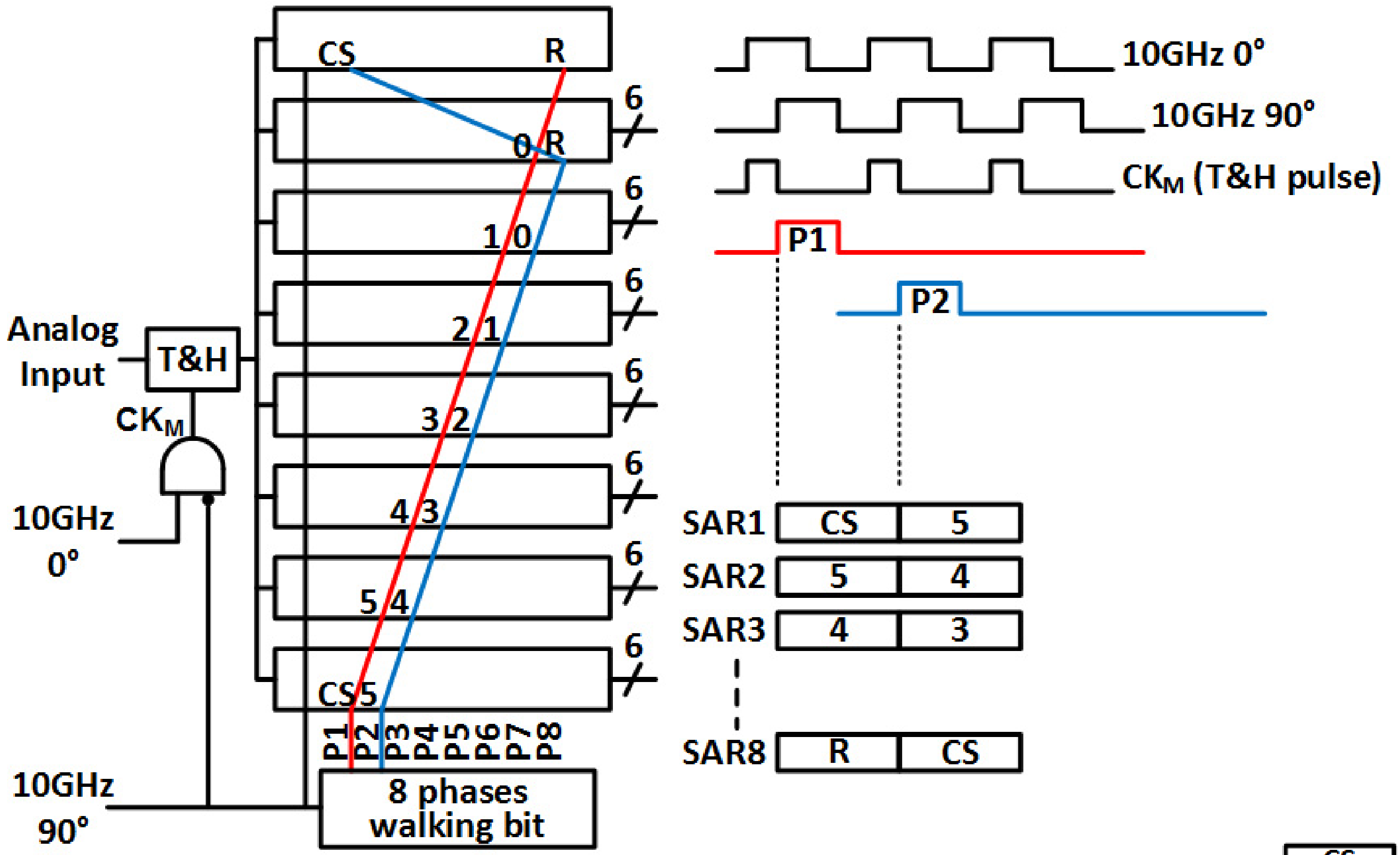
8x Time Interleaved SAR quantization



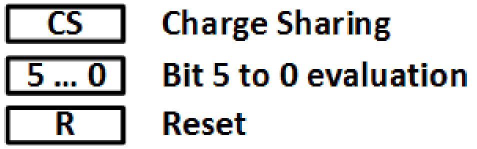
- 10GHz Synchronous quantization



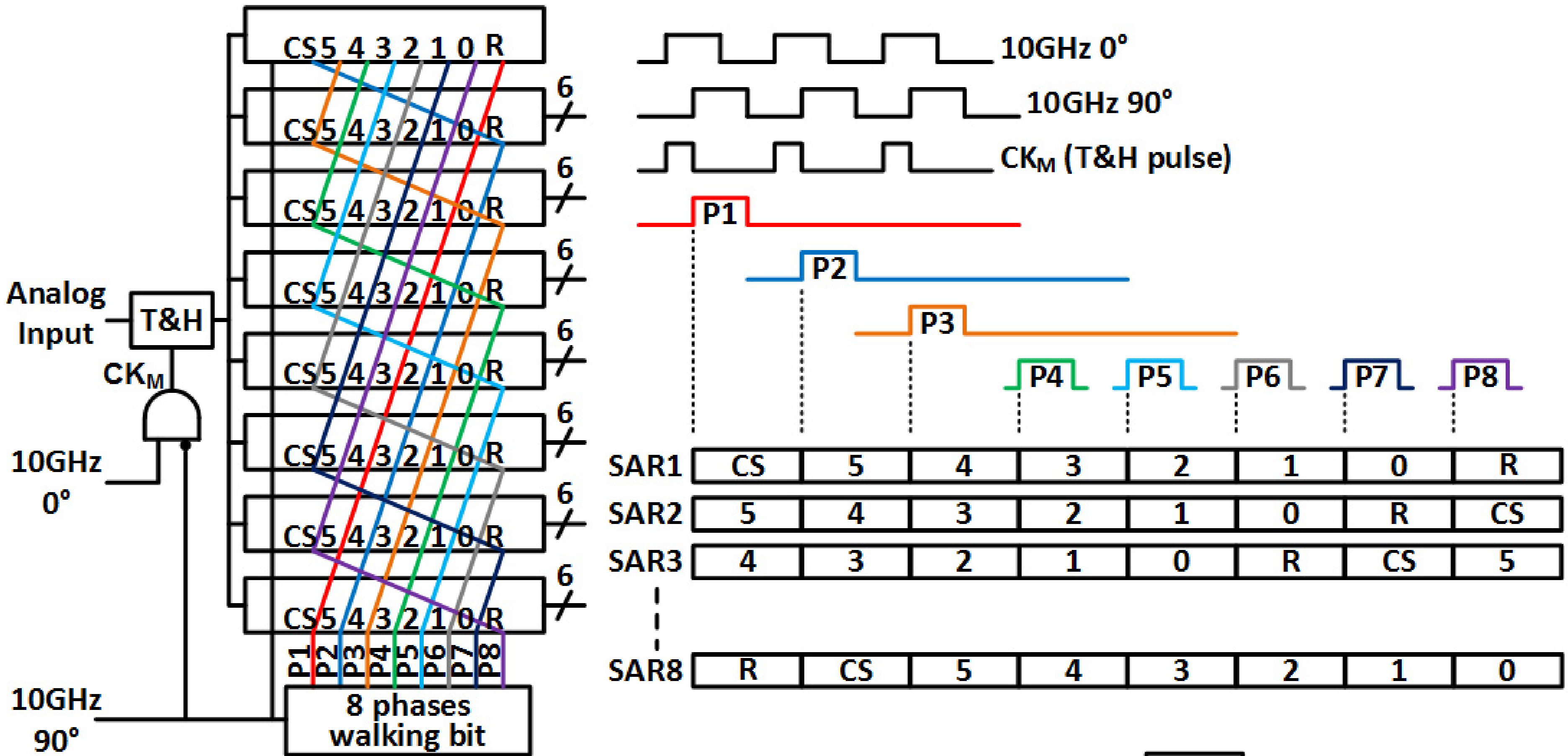
8x Time Interleaved SAR quantization



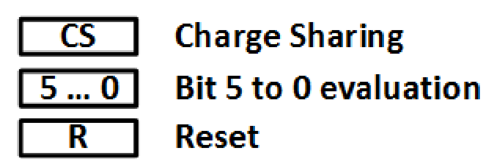
- 10GHz Synchronous quantization



8x Time Interleaved SAR quantization



- 10GHz Synchronous quantization



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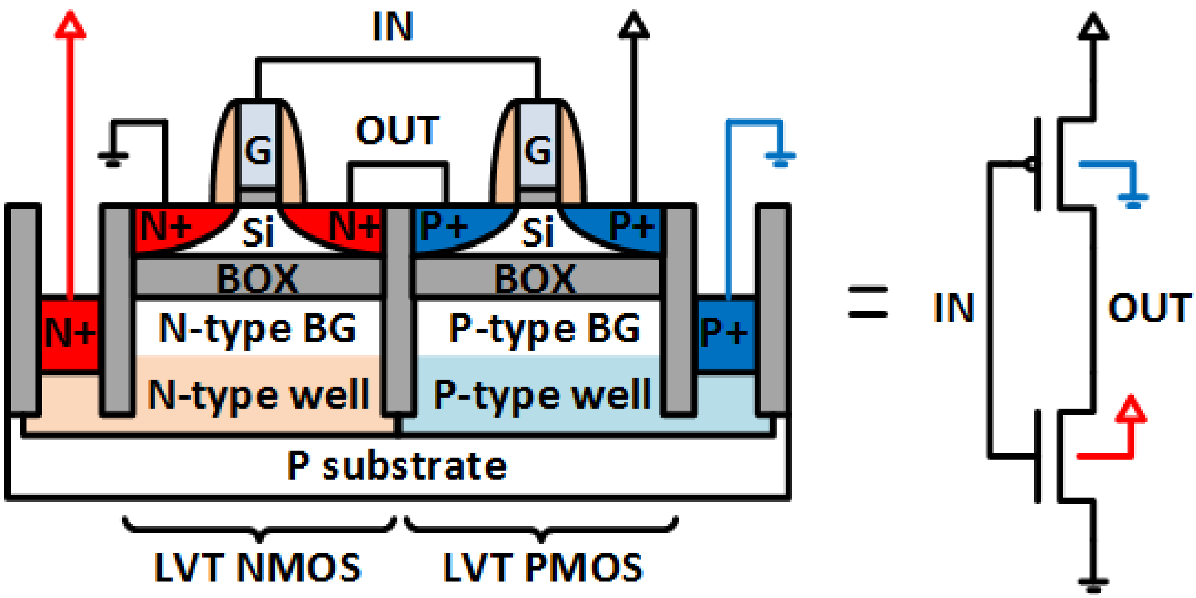
28nm UTBB FDSOI Technology



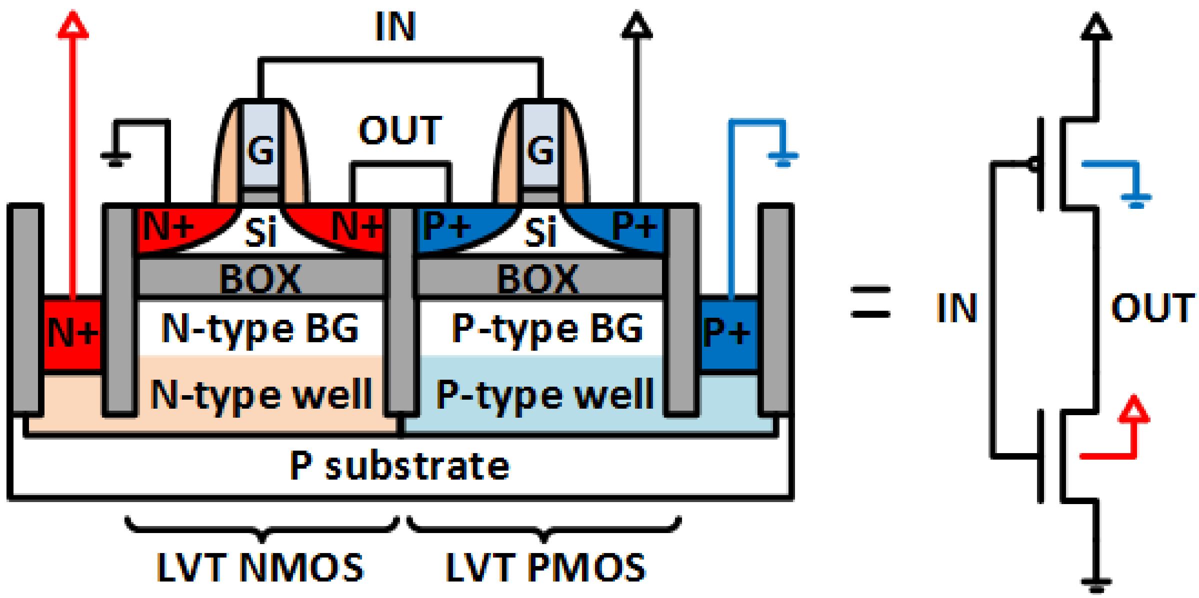
Si: Silicon film (7nm)

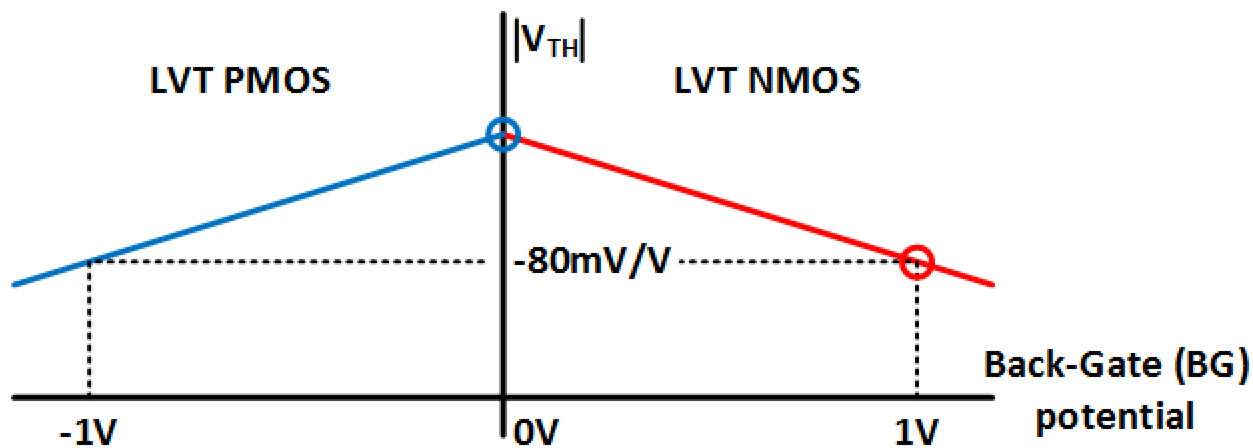
BOX: Buried Oxide (25nm)

BG: Back-Gate

(Drawing not to scale)

28nm UTBB FDSOI Technology





Si: Silicon film (7nm)

BOX: Buried Oxide (25nm)

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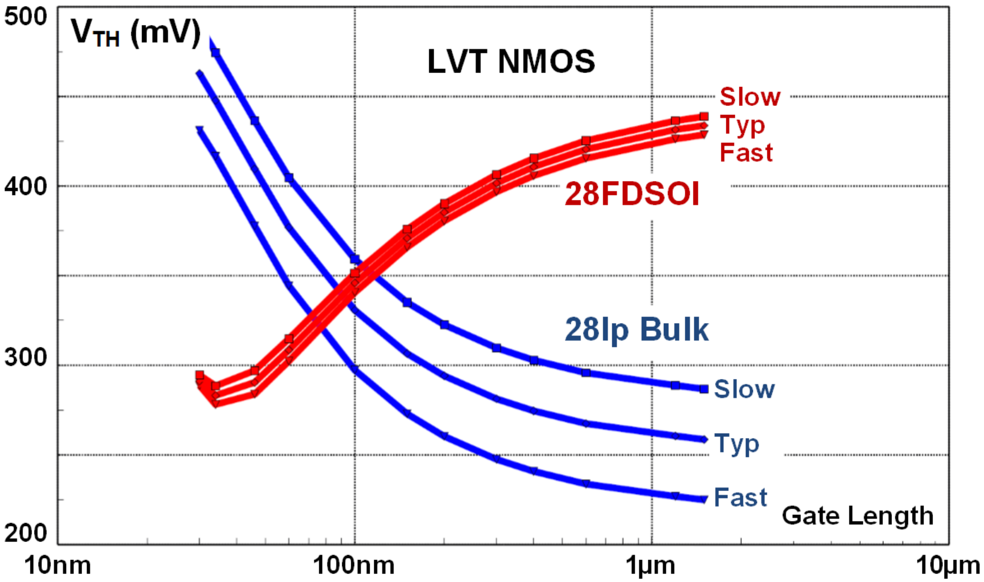
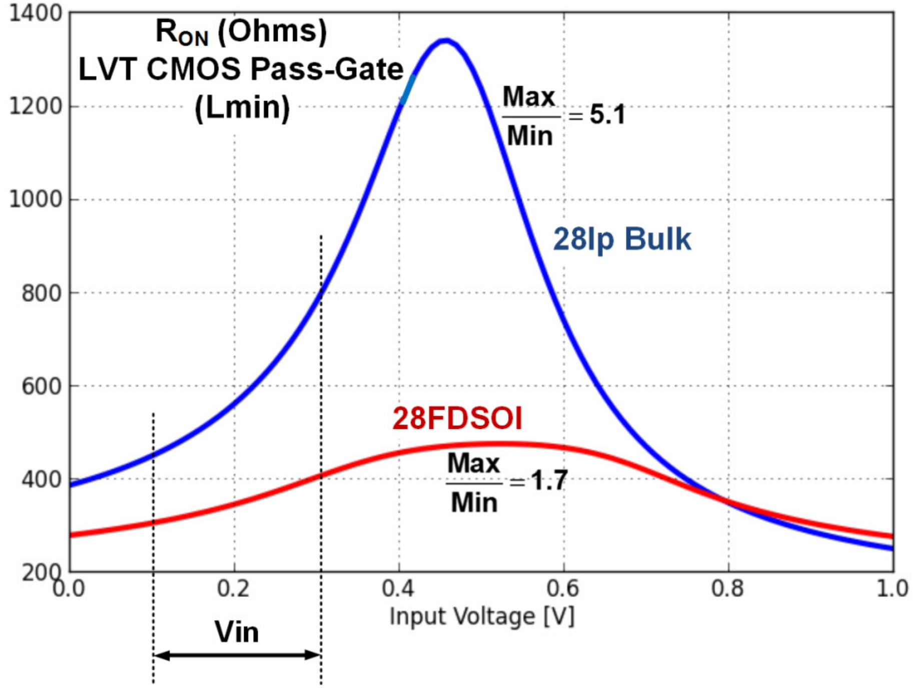
(Drawing not to scale)

28nm UTBB FDSOI for High-Speed SAR



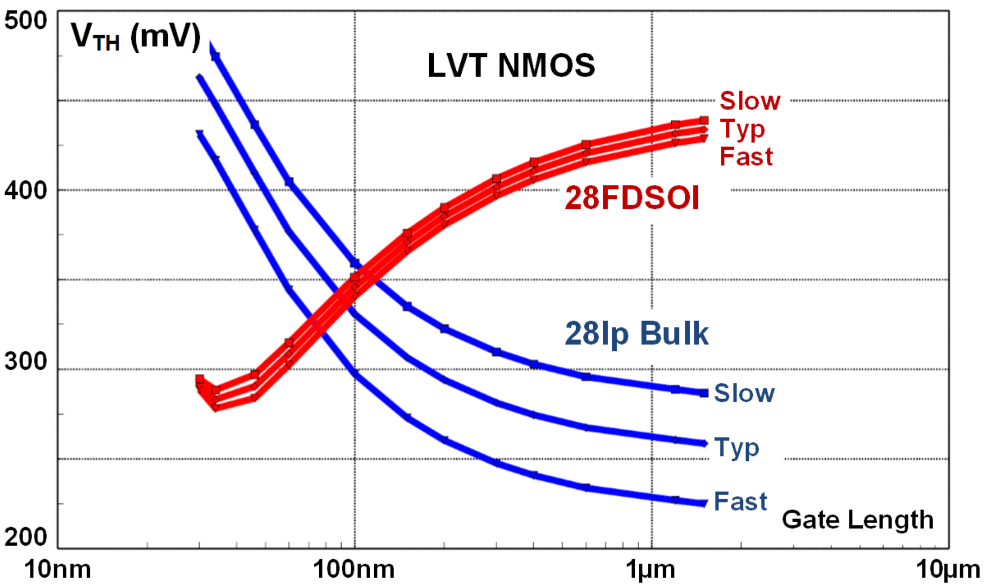


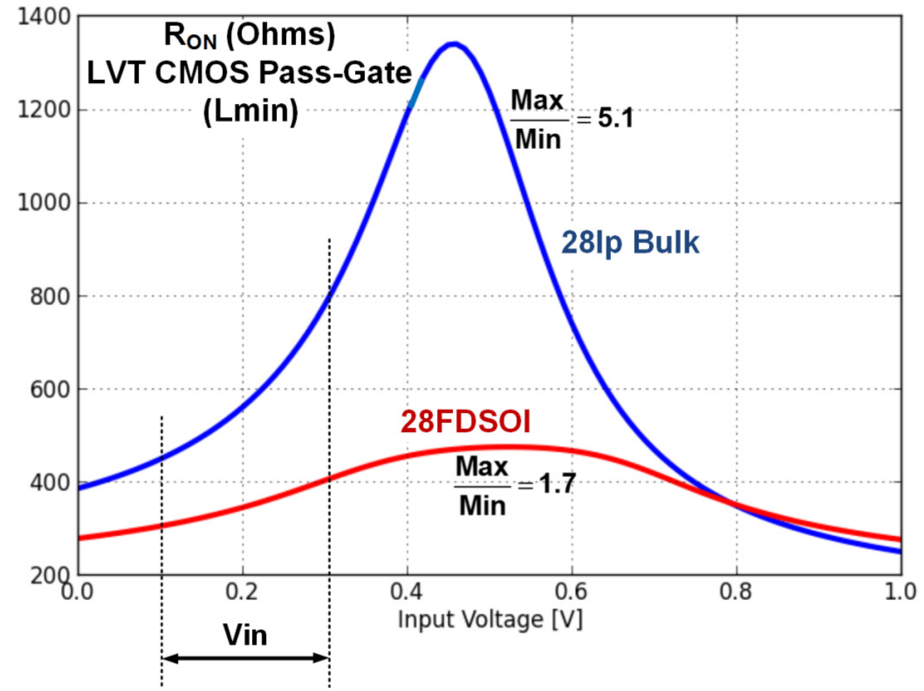
- <u>Lower Vth, less variability</u>

➢ Better switch: R_{ON} & linearity

➢ Faster logic

28nm UTBB FDSOI for High-Speed SAR





- <u>Lower Vth, less variability</u>
  - ➢ Better switch: R_{ON} & linearity
  - ➢ Faster logic

- <u>Reduced S/D capacitances</u>
  - ➢ Increased comparator BW
  - ➢ Reduced switch parasitics

Outline

- Architecture
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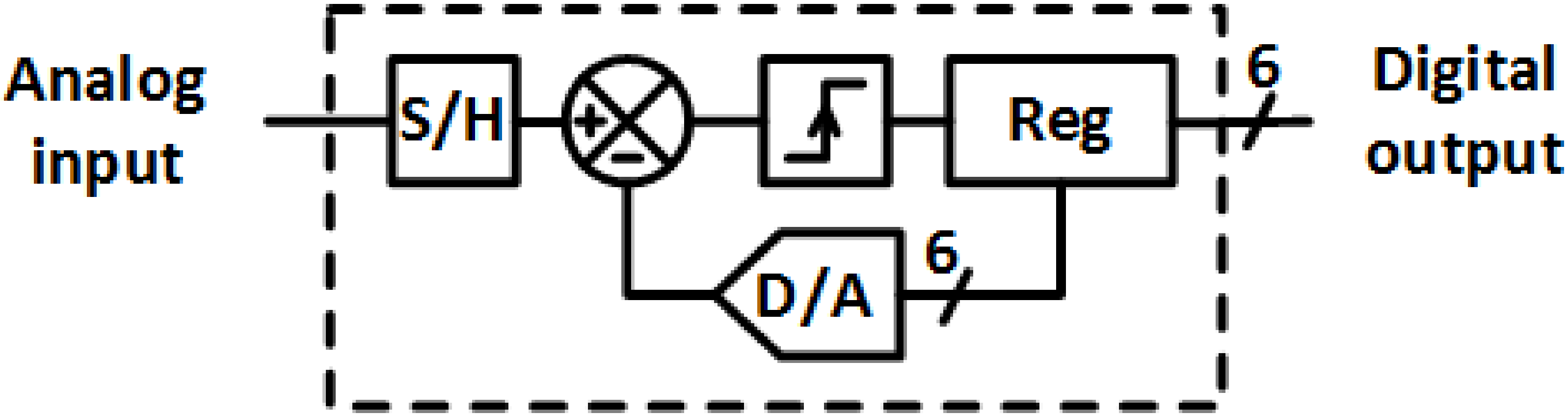
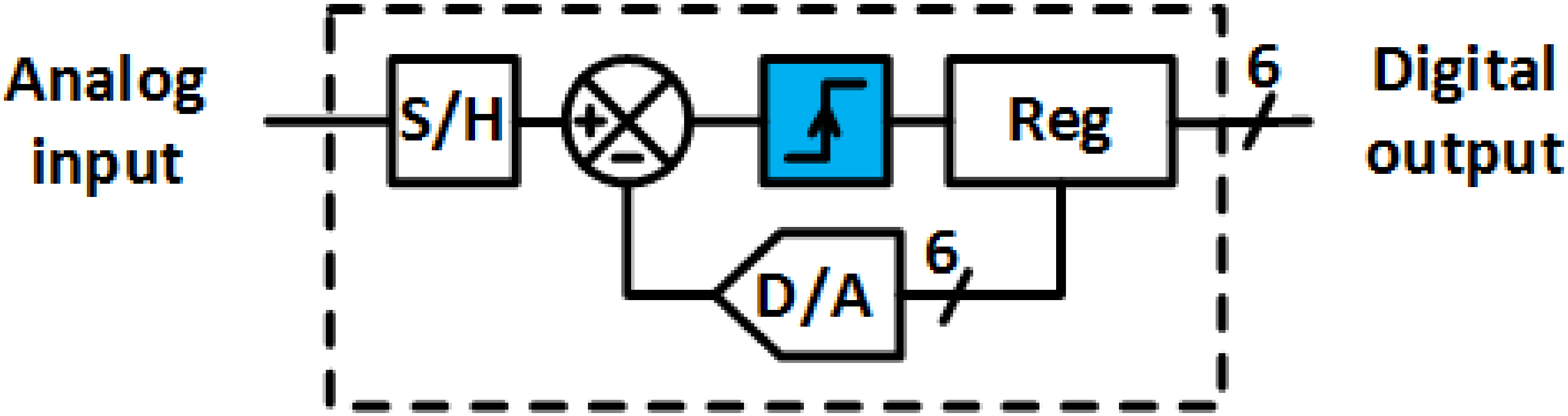
SAR overview



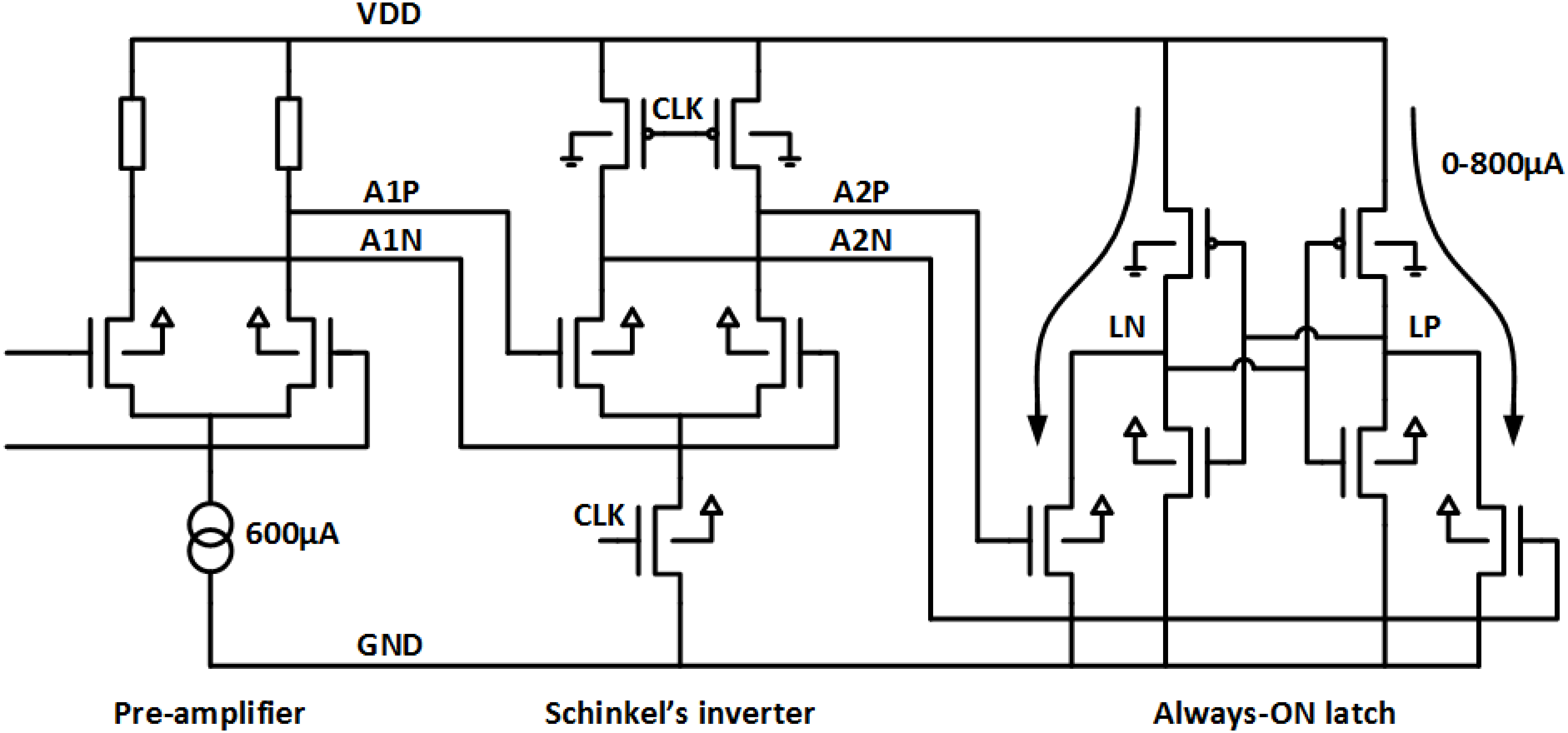
1975 McCreary & Gray
Conceptual Successive Approximation ADC

SAR overview



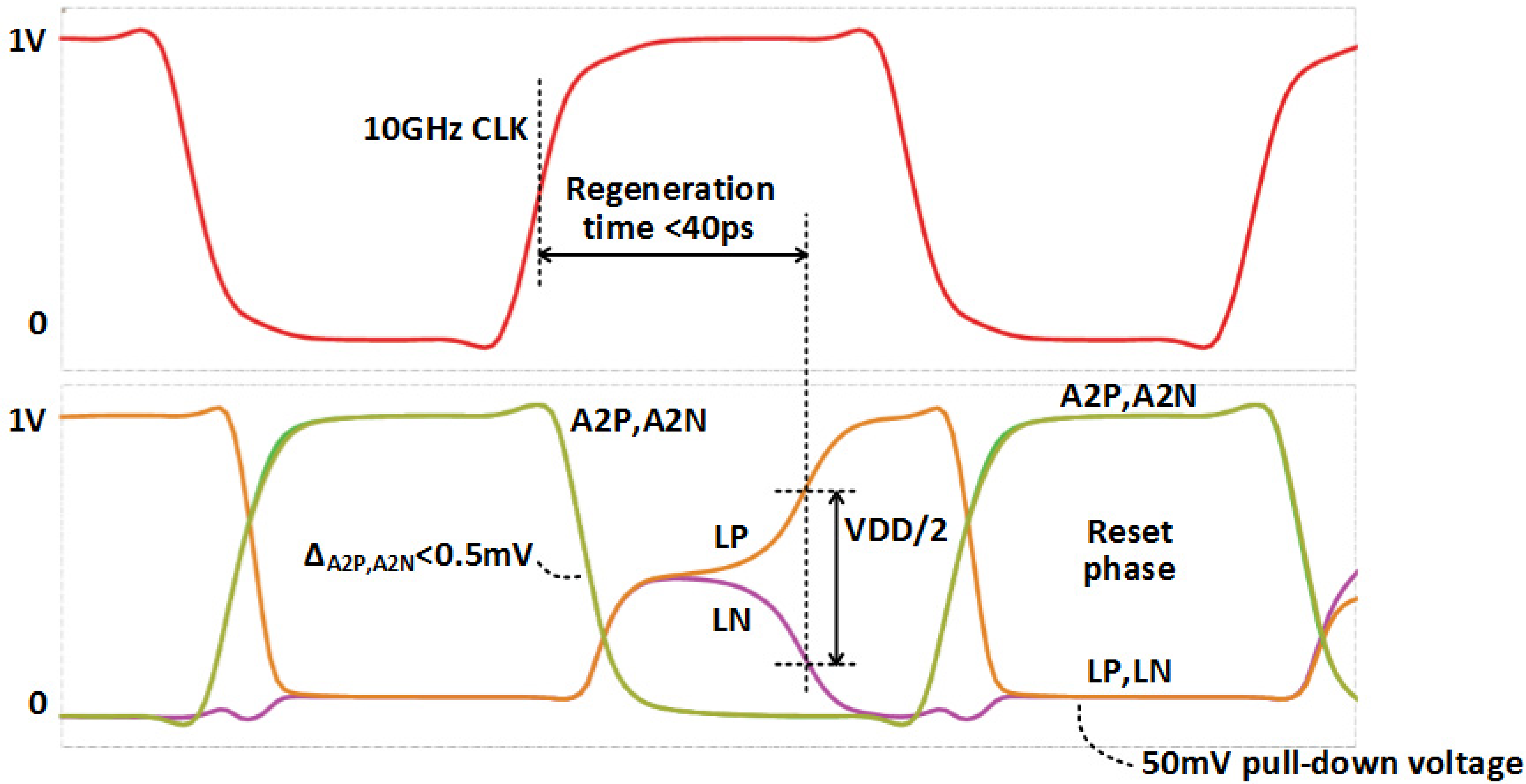
1975 McCreary & Gray
Conceptual Successive Approximation ADC

Comparator and latch



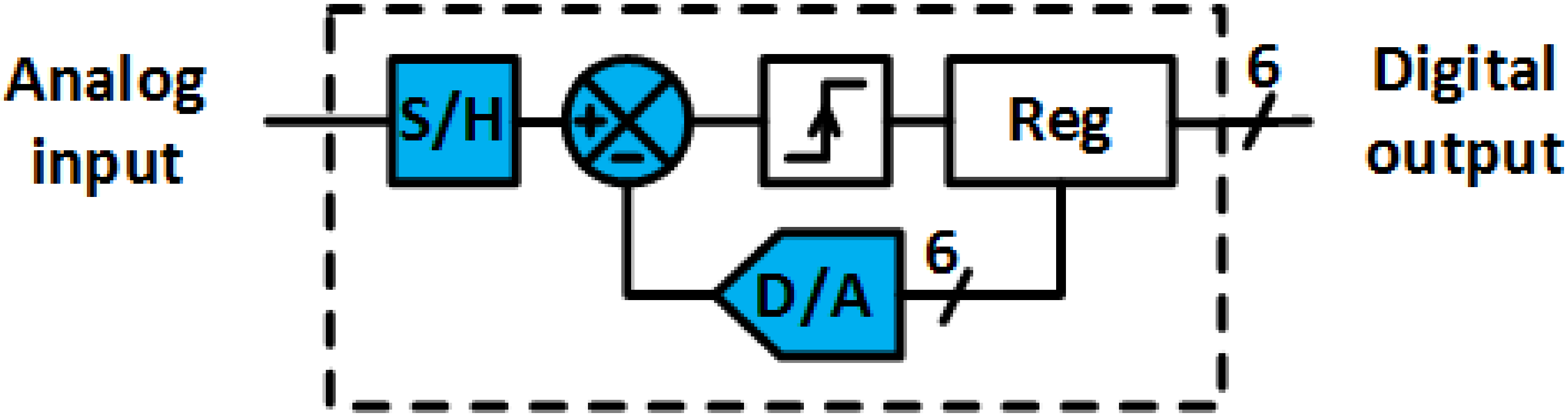
- >30GHz internal bandwidth
- $1mV_{RMS}$ input referred noise (limits final SNR)
- 1.8mW

Comparator and latch



- <1/10th LSB regeneration capability

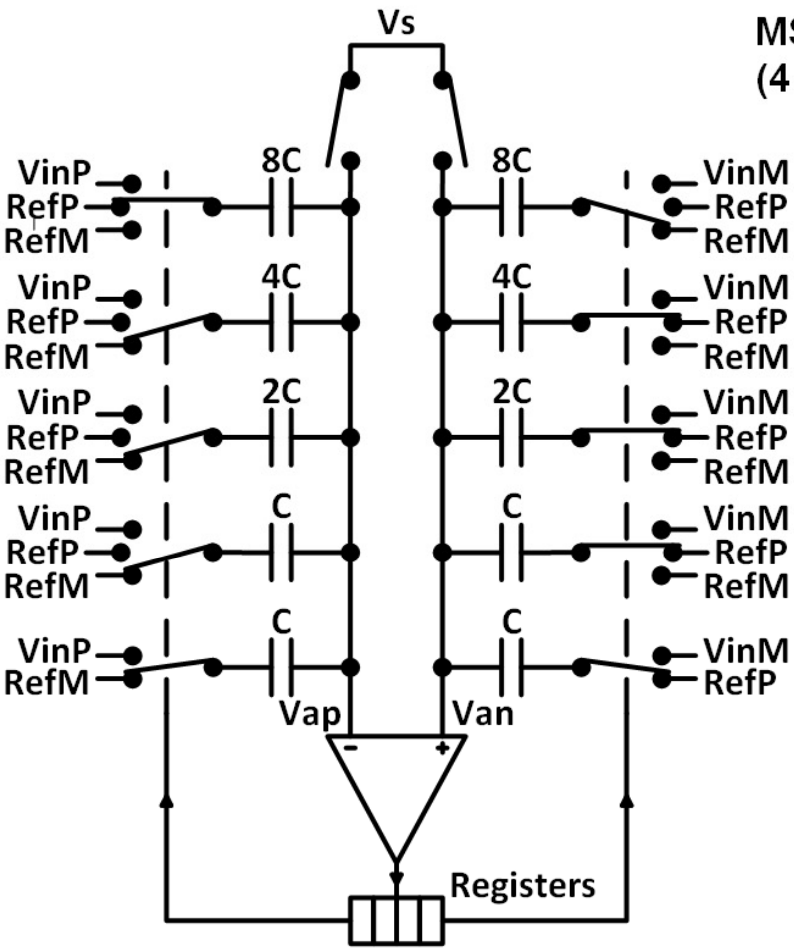
SAR overview



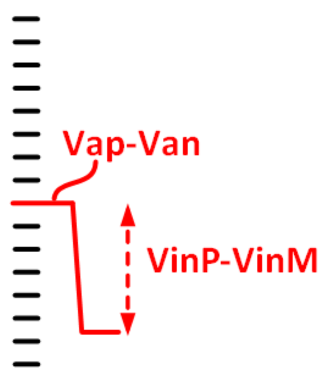
1975 McCreary & Gray
Conceptual Successive Approximation ADC

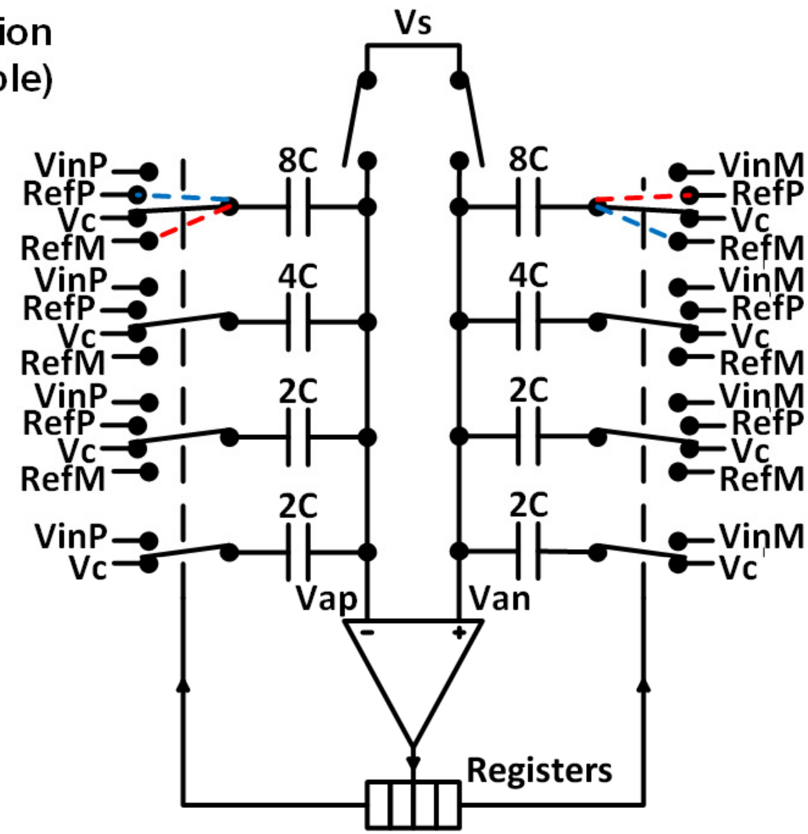
Charge Redistribution

MSB Evaluation
(4 bits example)



2 References
Conventional « Set & Correct » algorithm

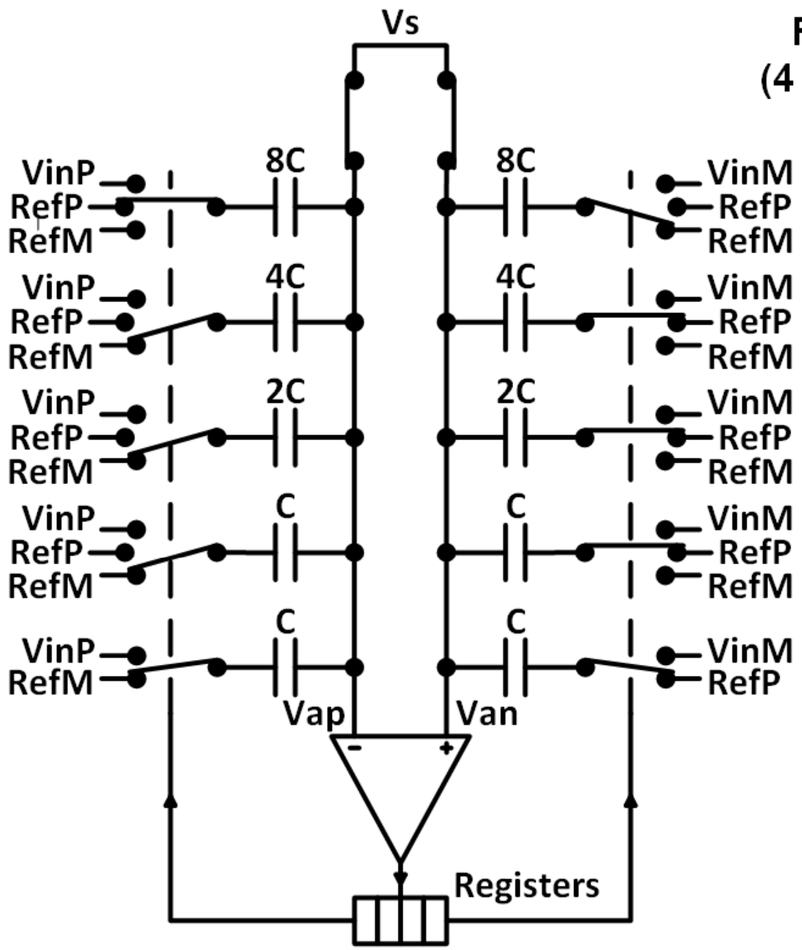




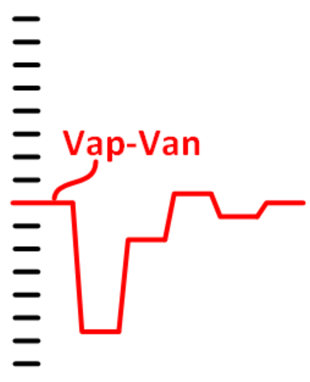
2+1 References
« Decide right » algorithm
Used in this chip

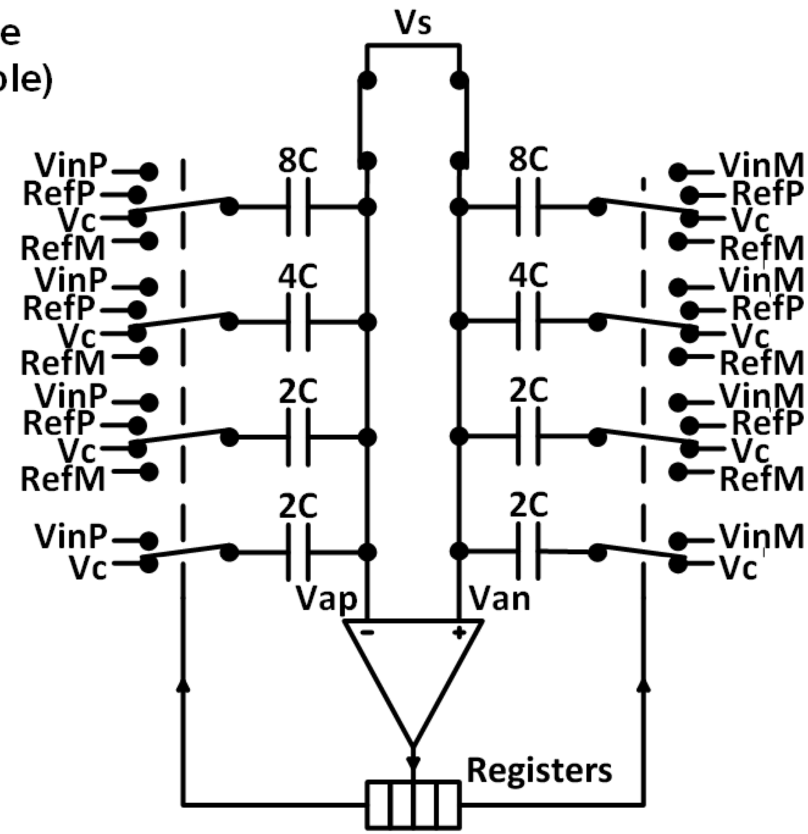
Charge Redistribution

Reset phase
(4 bits example)



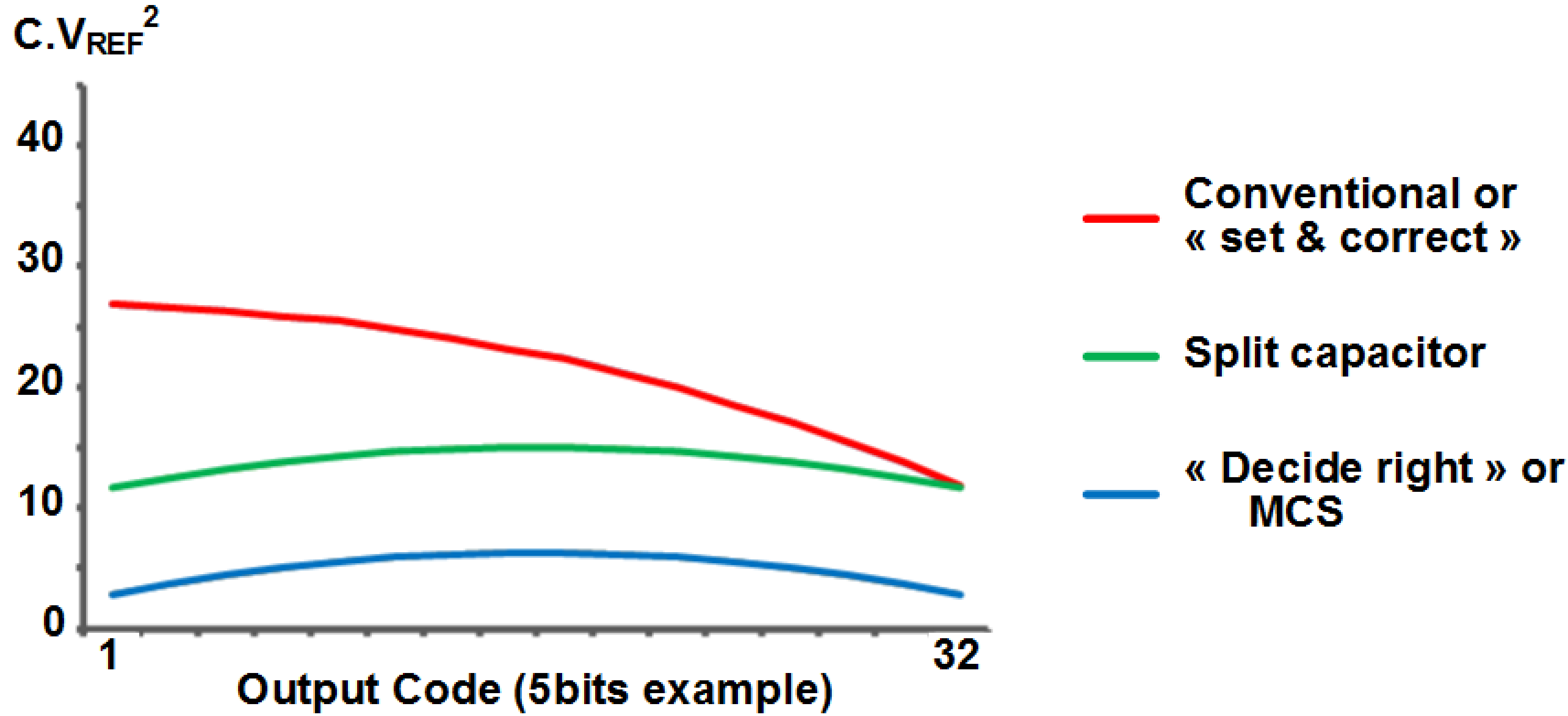
2 References
Conventional « Set & Correct » algorithm





2+1 References
« Decide right » algorithm
Used in this chip

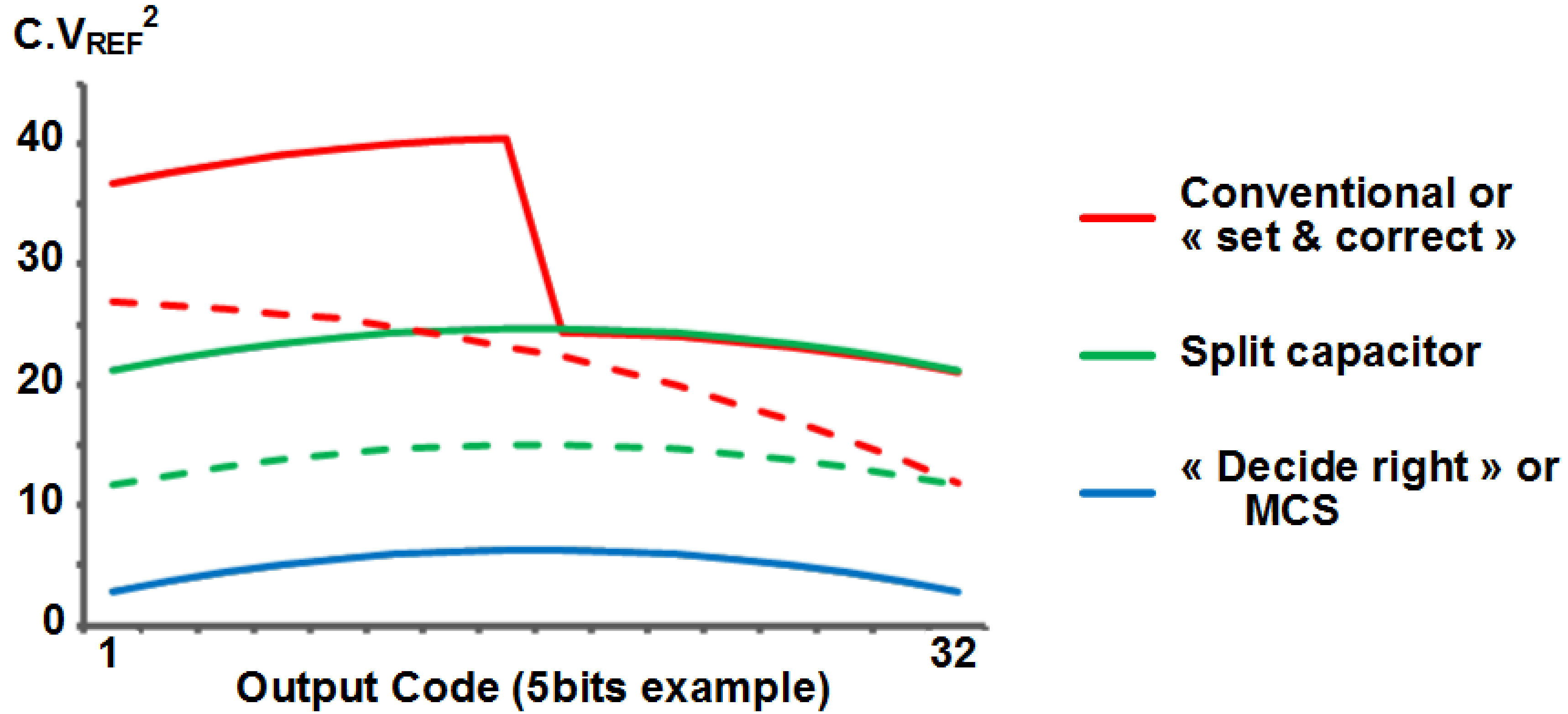
Switching energy (quantization only)



[Hariprasath & Al., Electronics Letters, Apr. 2010]

[Zhu & Al., JSSC, June 2010]

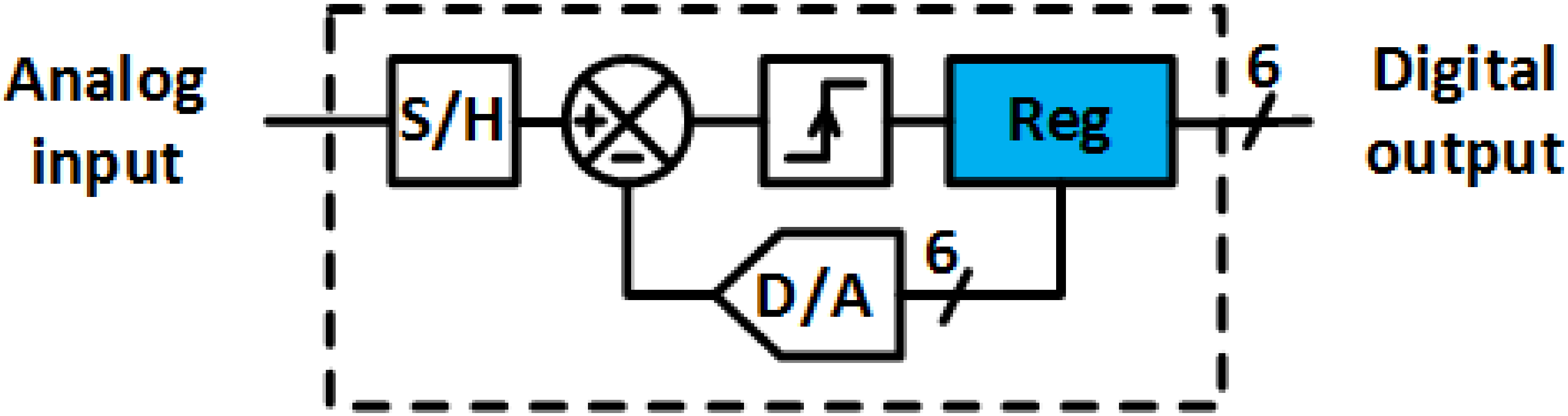
Switching energy (with reset)



[Hariprasath & Al., Electronics Letters, Apr. 2010]

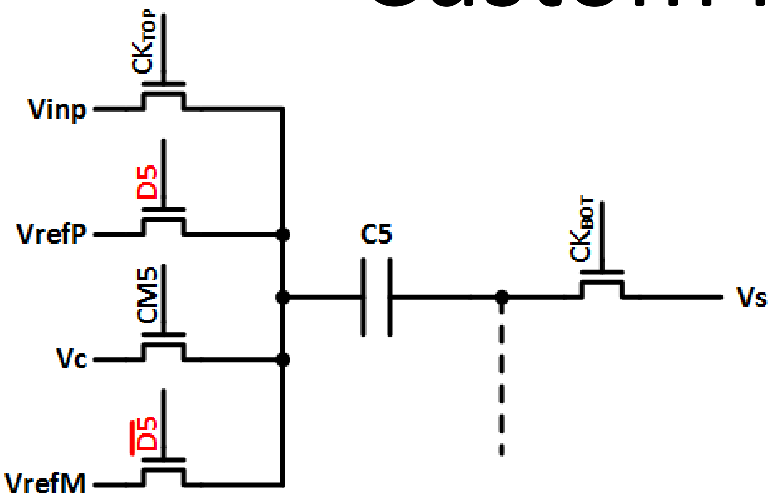
[Zhu & Al., JSSC, June 2010]

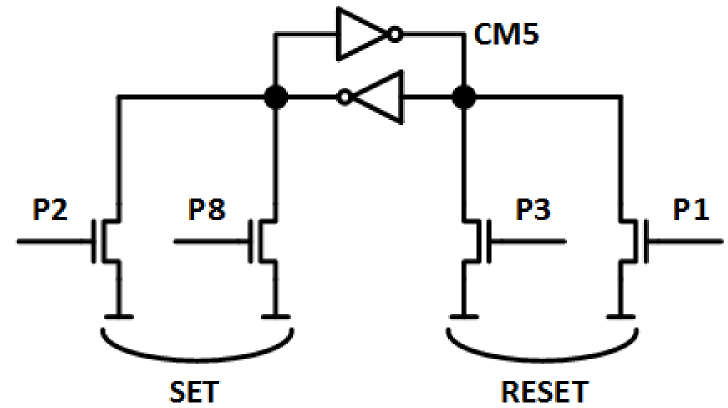
SAR overview

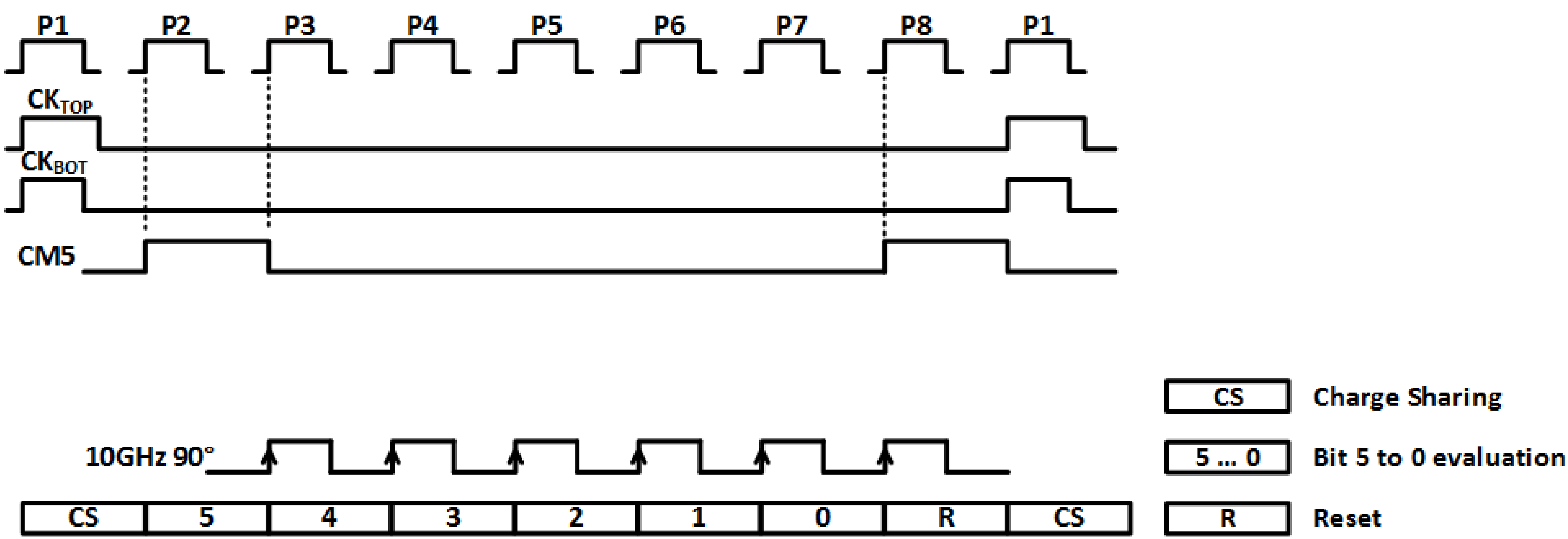


1975 McCreary & Gray
Conceptual Successive Approximation ADC

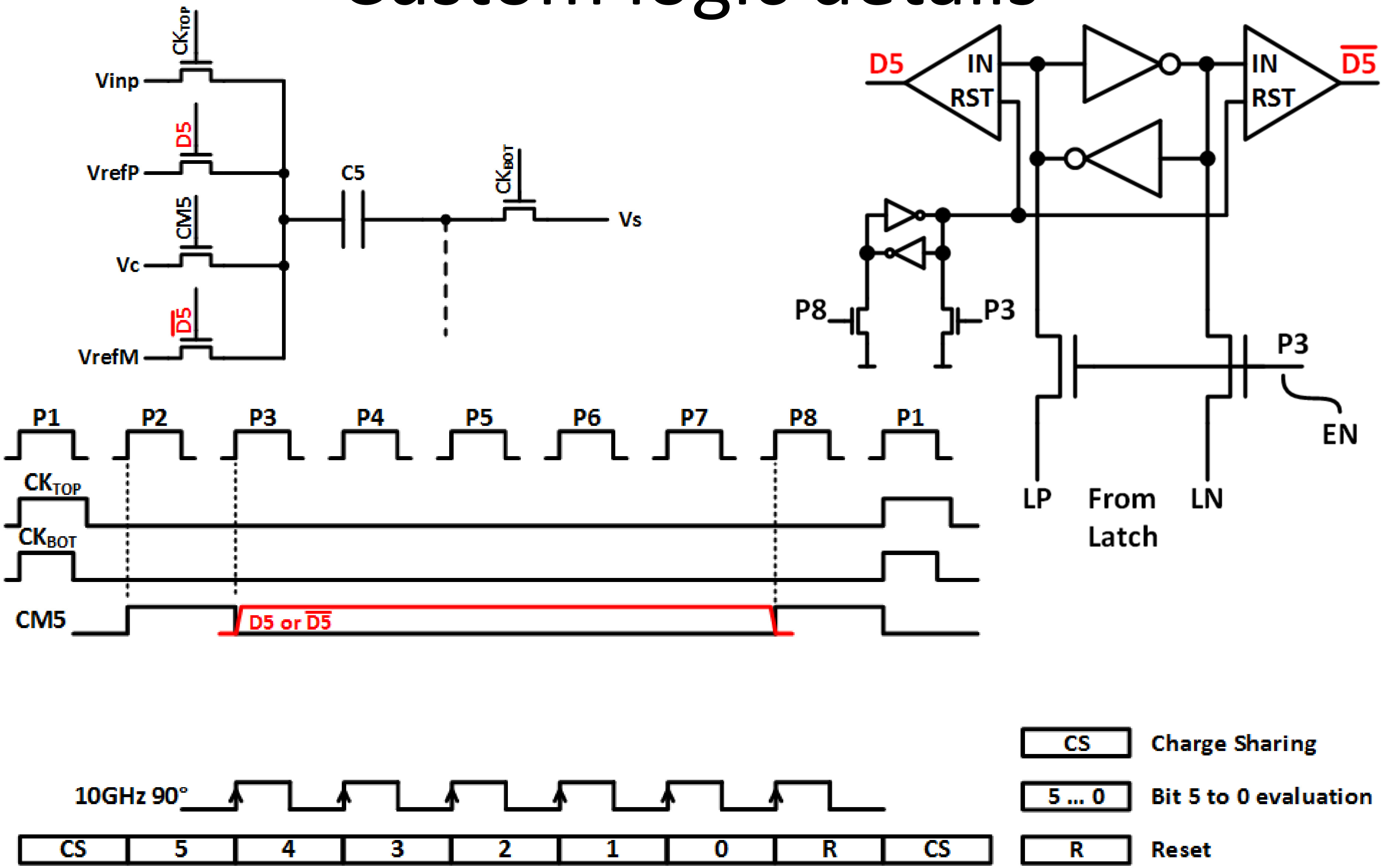
Custom logic details



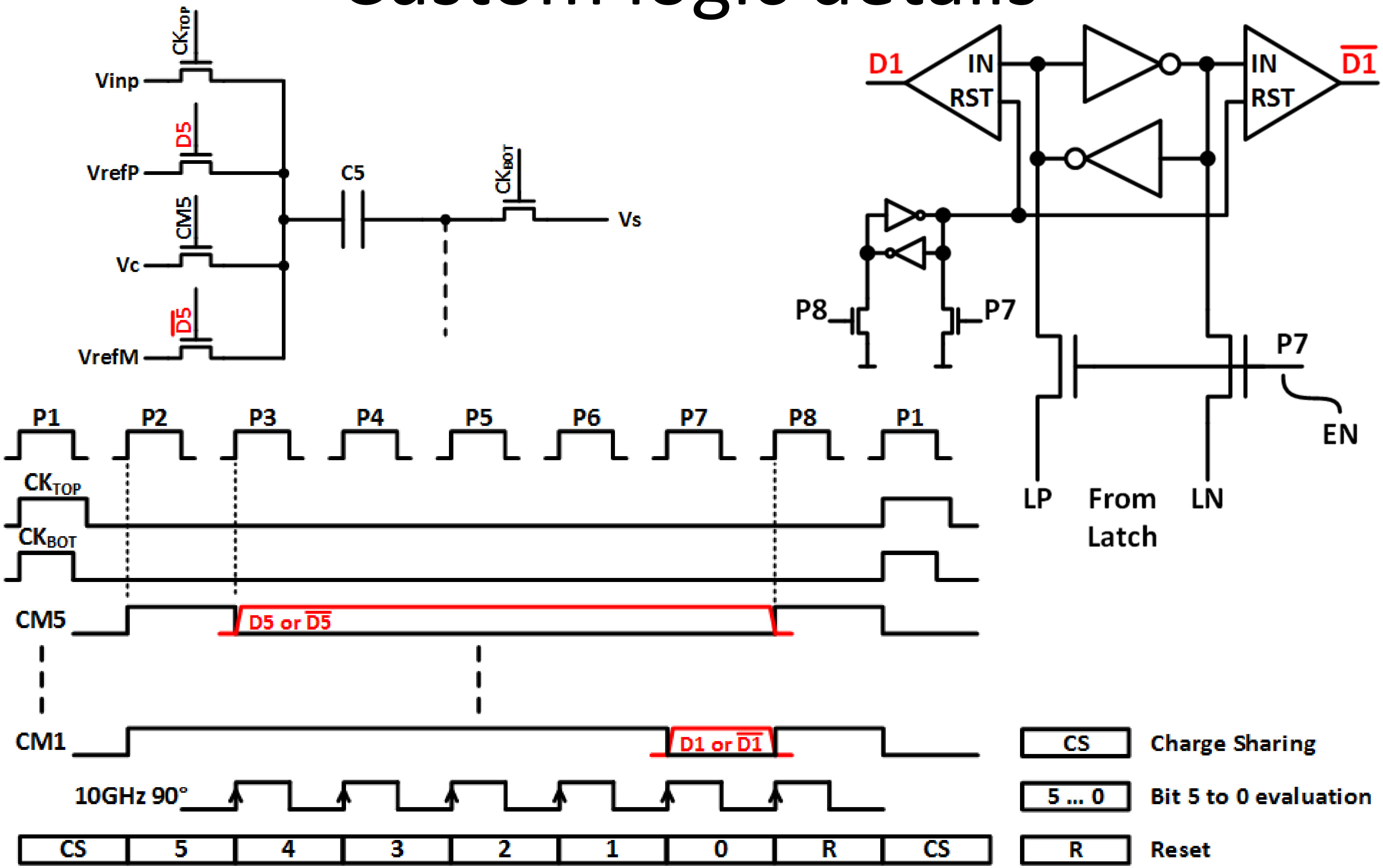




Custom logic details



Custom logic details



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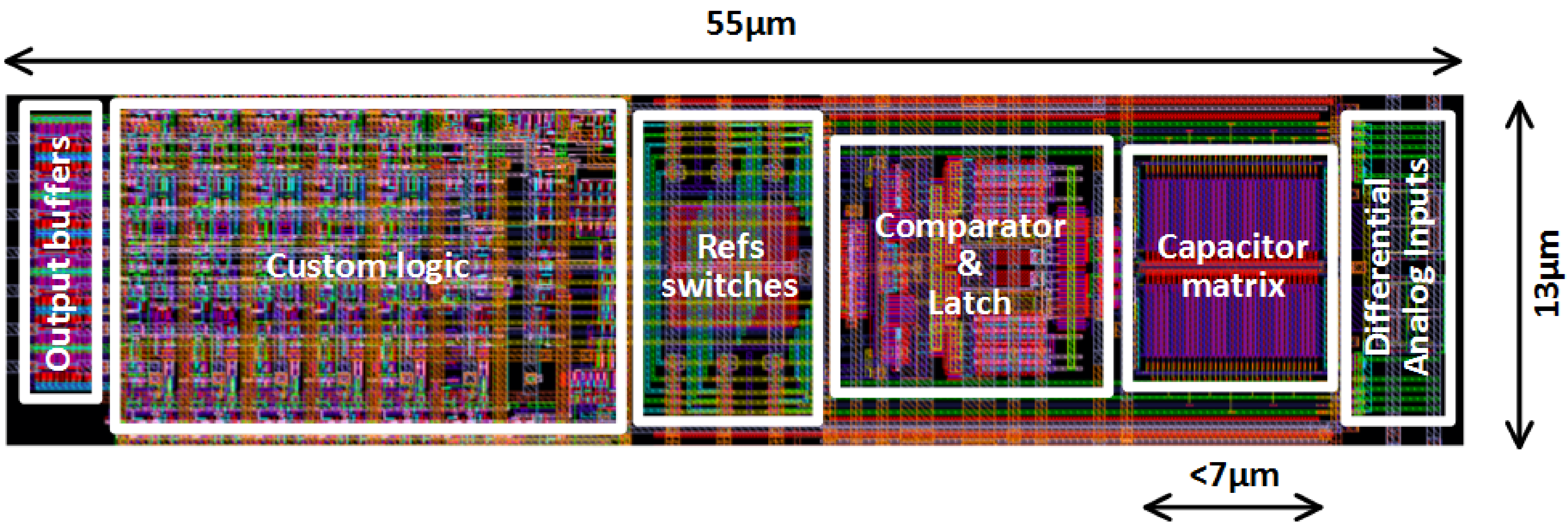
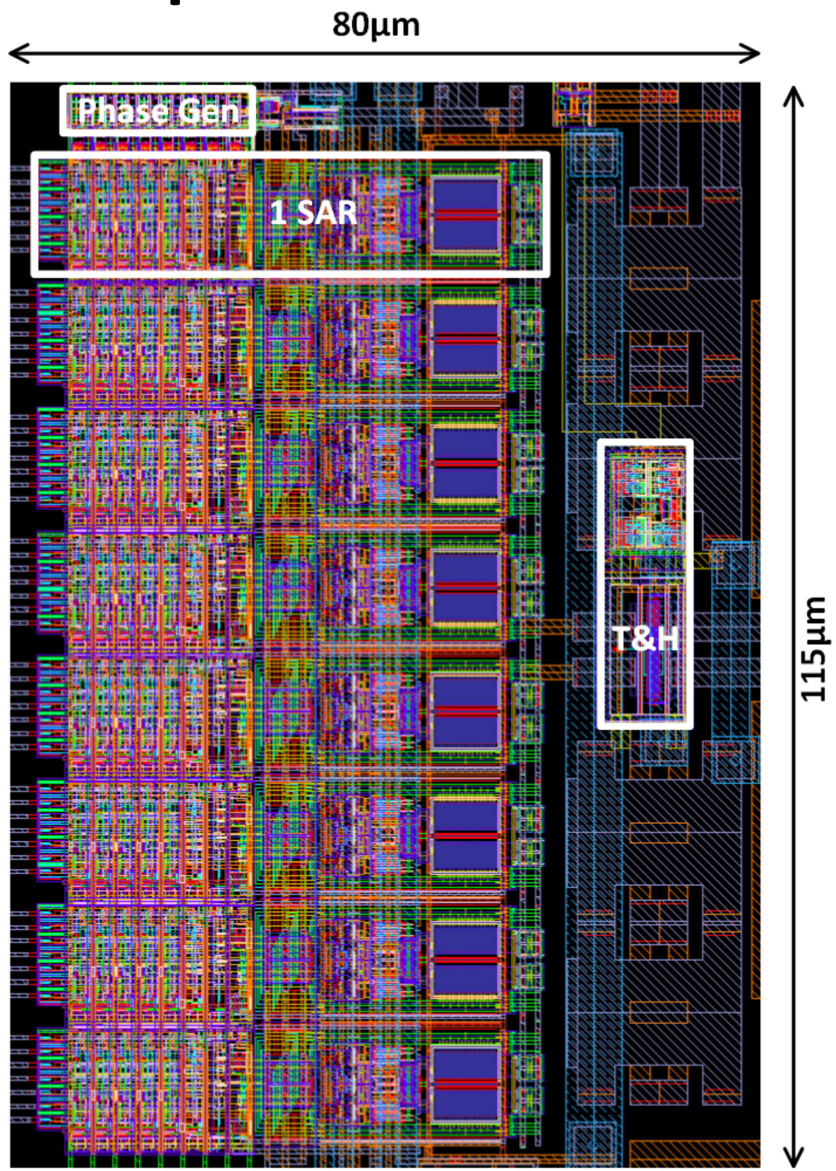
1 SAR slice

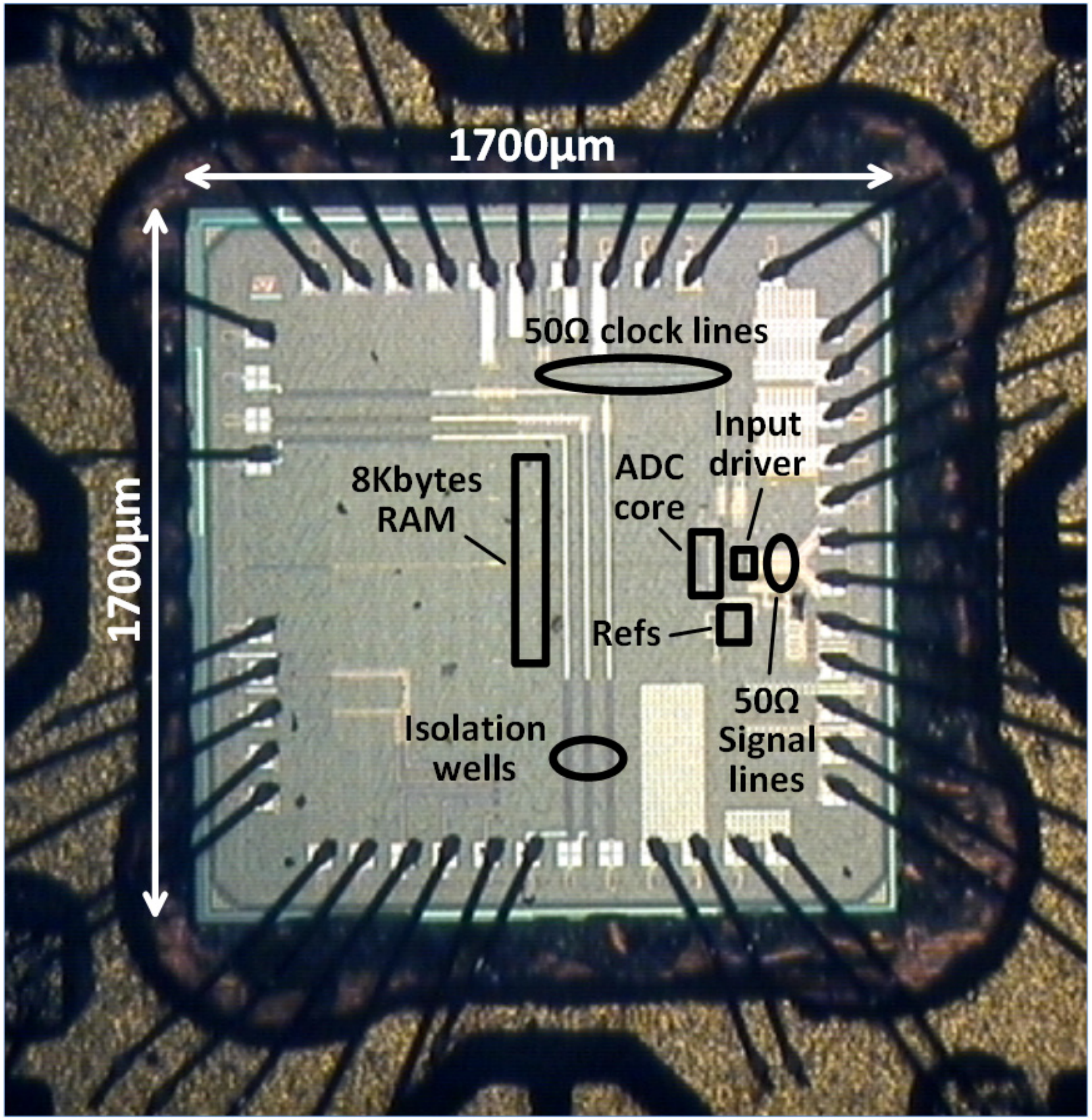


- Minimum pitch capacitor matrix
- Custom layout logic
- ➢ Reduced propagation length

Complete ADC core



Die mounted in its chip-on-board cavity



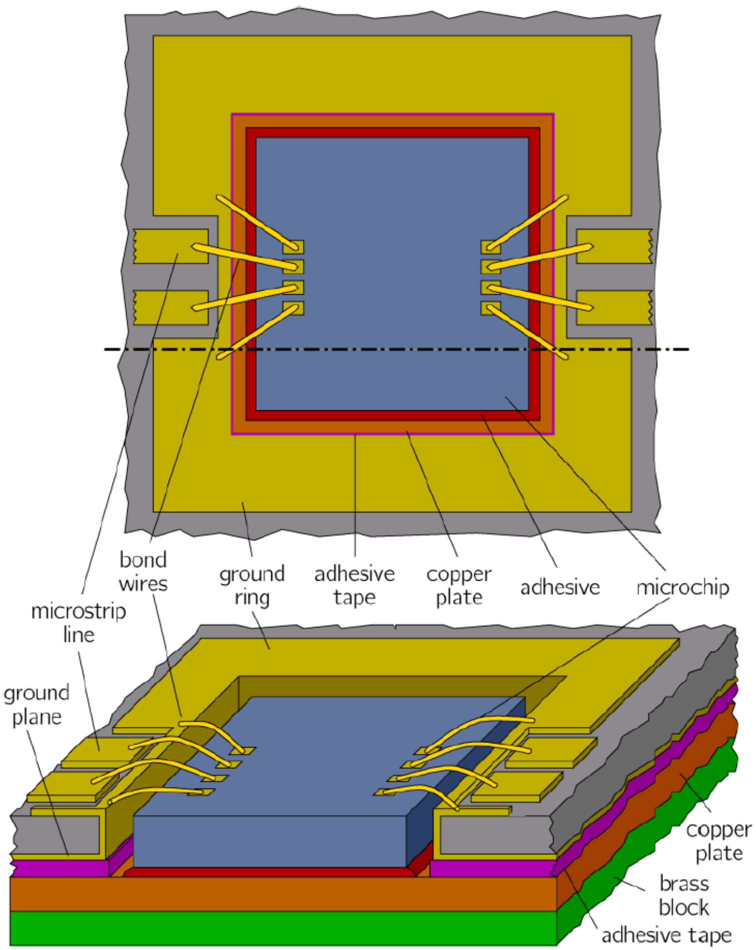
Process:

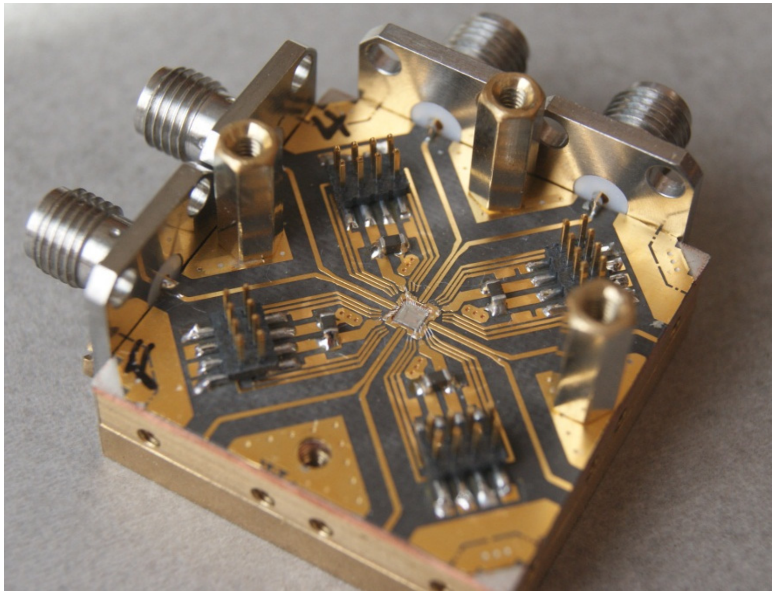
ST 28nm UTBB FDSOI

ADC core area:

0.009mm^2

Module assembly





SMA-input to line-end:

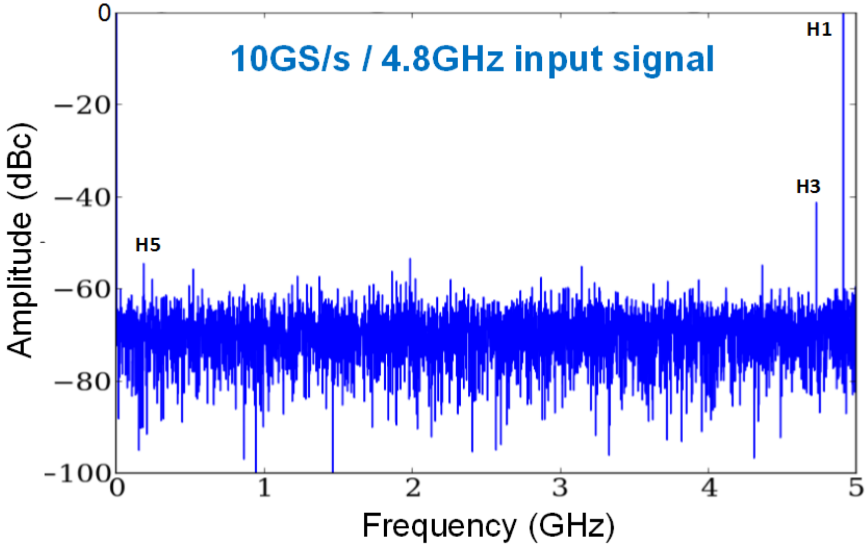
- Less than 2.5dB losses from 1 to 20GHz

Courtesy Philipp Ritter, Saarland University, Germany

Outline

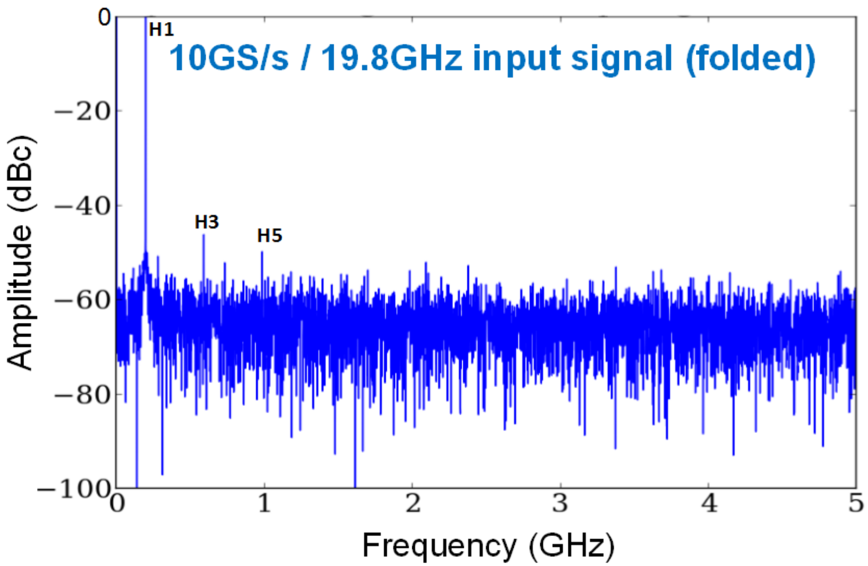
- Architecture
- Technology
- Design details
- Layout
- Module assembly
- **Measurements**
- Conclusion

10GS/s output spectrum



SNR=34.27dB
THD=40.93dB
SFDR=41.11dB
SINAD=33.75dB / ENOB=5.31
Output Amplitude = -2.85dBFS
Offset is calibrated off-chip

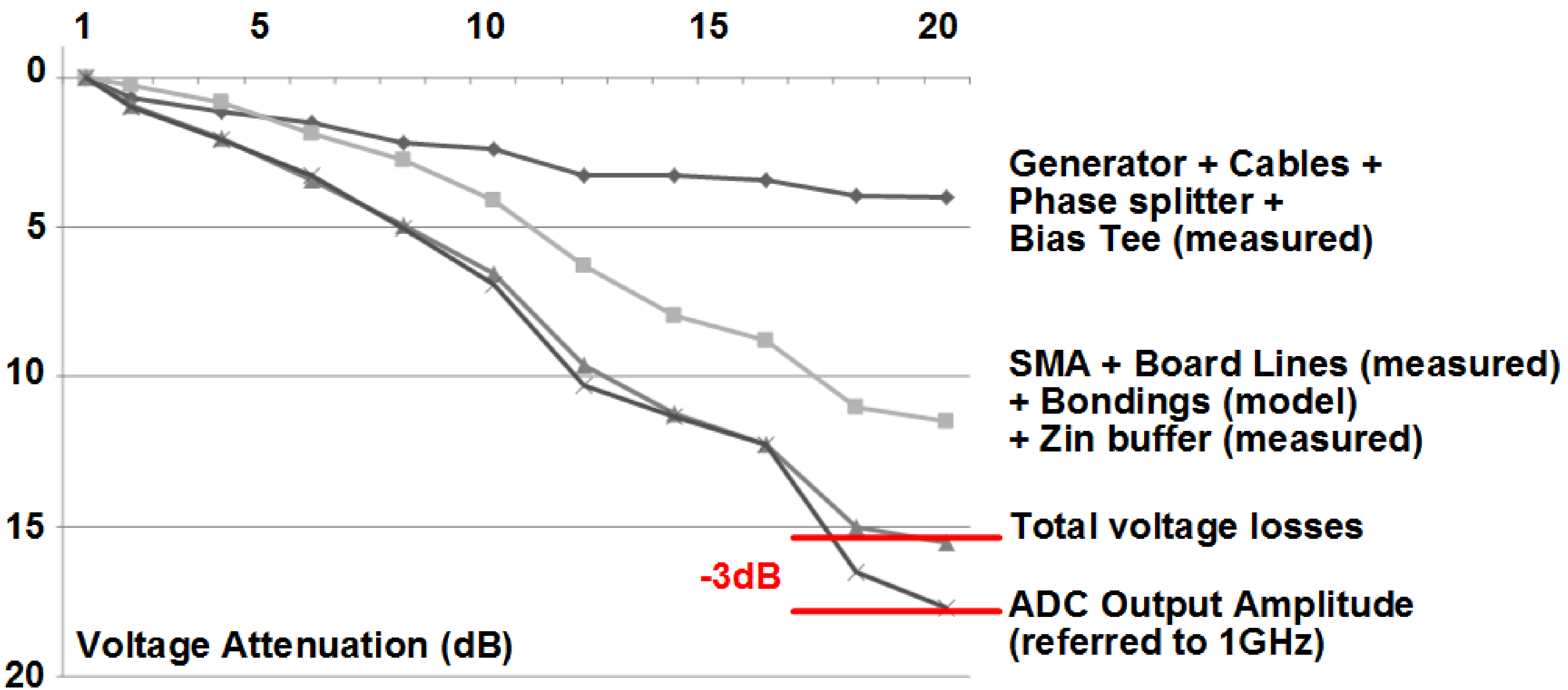
Thermal noise limited (Comparator & Latch)



SNR=29.79dB
THD=44.24dB
SFDR=46.11dB
SINAD=29.69dB / ENOB=4.64
Output Amplitude = -3.07dBFS
Offset is calibrated off-chip

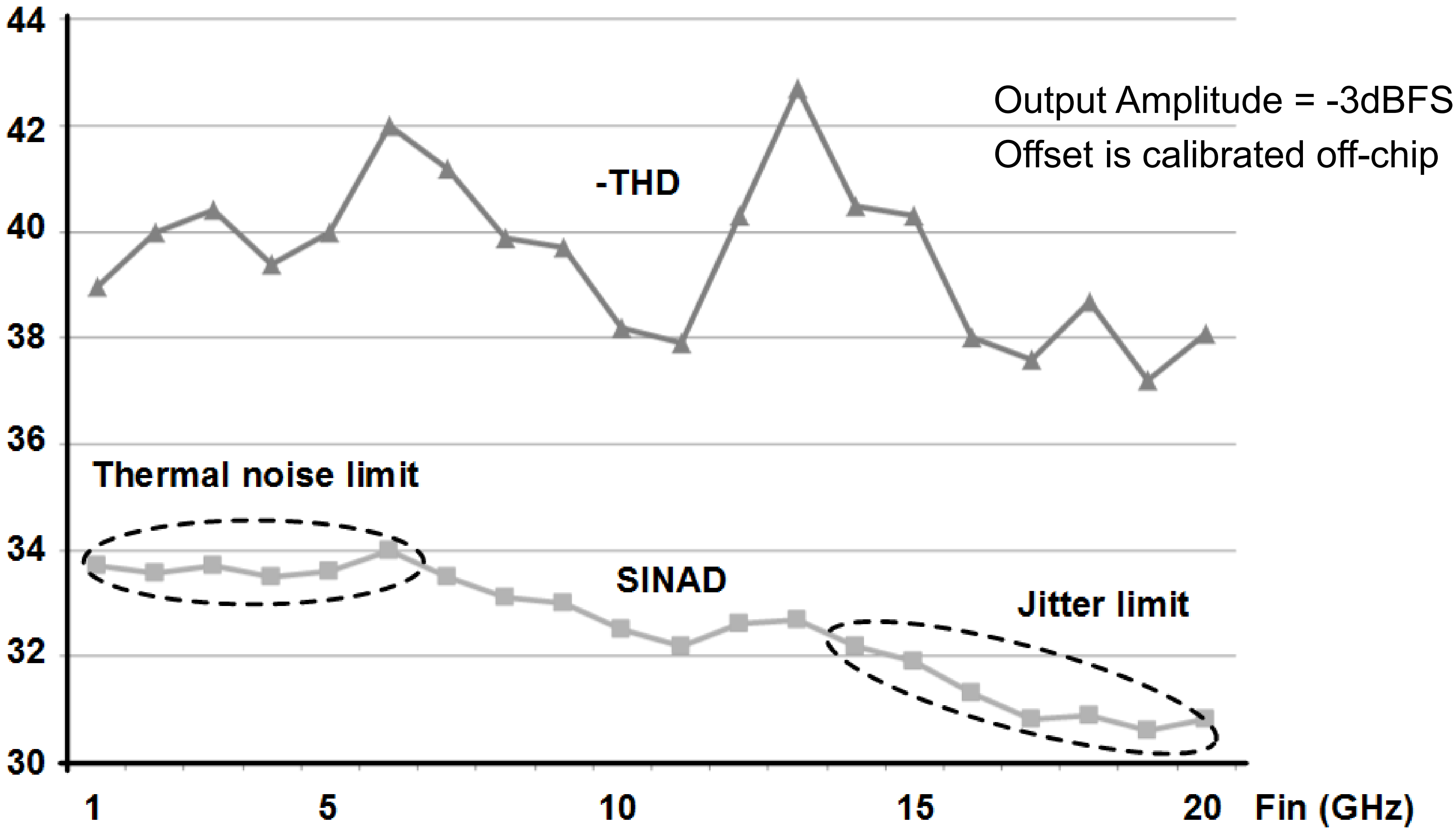
Jitter limited (about $260fs_{rms}$ incl. Generator)

Input frequency response



- Actual bandwidth (de-embedded) is 20GHz

Input frequency response



Performance summary

	Verma ISSCC 2013	Tabasy VLSI 2013	Kull VLSI 2013	This Work
Technology	40nm CMOS	65nm CMOS	32nm SOI	**28nm UTBB FDSOI**
Architecture	TI-FLASH	TI-SAR	TI-SAR	**TI-SAR**
Power Supply (V)	0.9	1.1 / 0.9	1	**1**
Sampling Rate (GS/s)	10.3	10	8.8	**10**
Resolution (bits)	6	6	8	**6**
Power Consumption (mW)	240	79.1	35	**32**
SNDR @ Nyquist (dB)	33	26	38.5	**33.8**
Active Area (mm^2)	0.27	0.33	0.025	**0.009**
FOM @ Nyquist (fJ/conv)	700	480	58	**81**
Max Input Frequency (GHz)	6	4.5	4.2	**20**
Gain/Skew Calibration	Yes	Yes	Yes	**No**

Conclusion

- Demonstration of :
  - 10GSps operation
    - Master T&H
    - 6b synchronous quantization
  - Enabled by :
    - Pure passive sample & redistribute concept
    - NMOS based design
      (sampling, comparator & latch, custom logic)
    - 28nm UTBB FDSOI speed capability
- Making this ADC well suited for further higher speed interleaving (100Gb optical link)

Special thanks

- Dimitri Goguet (STMicroelectronics)
- Sébastien Pruvost (STMicroelectronics)
- Philipp Ritter (Saarland University)
- Alex Zabroda (Consultant, previously with STM)

A 1GS/s 10b 18.9mW Time-interleaved SAR ADC with Background Timing Skew Calibration

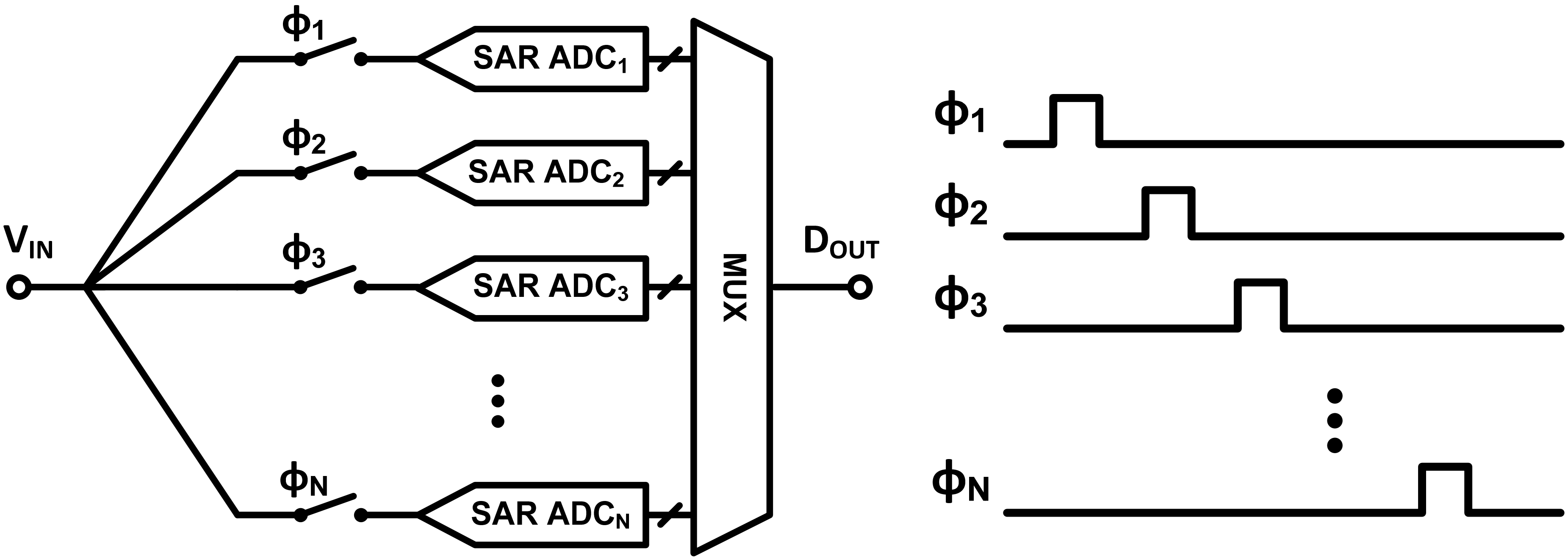
Sunghyuk Lee,
Anantha P. Chandrakasan, Hae-Seung Lee

MIT, Cambridge, MA, USA

Outline

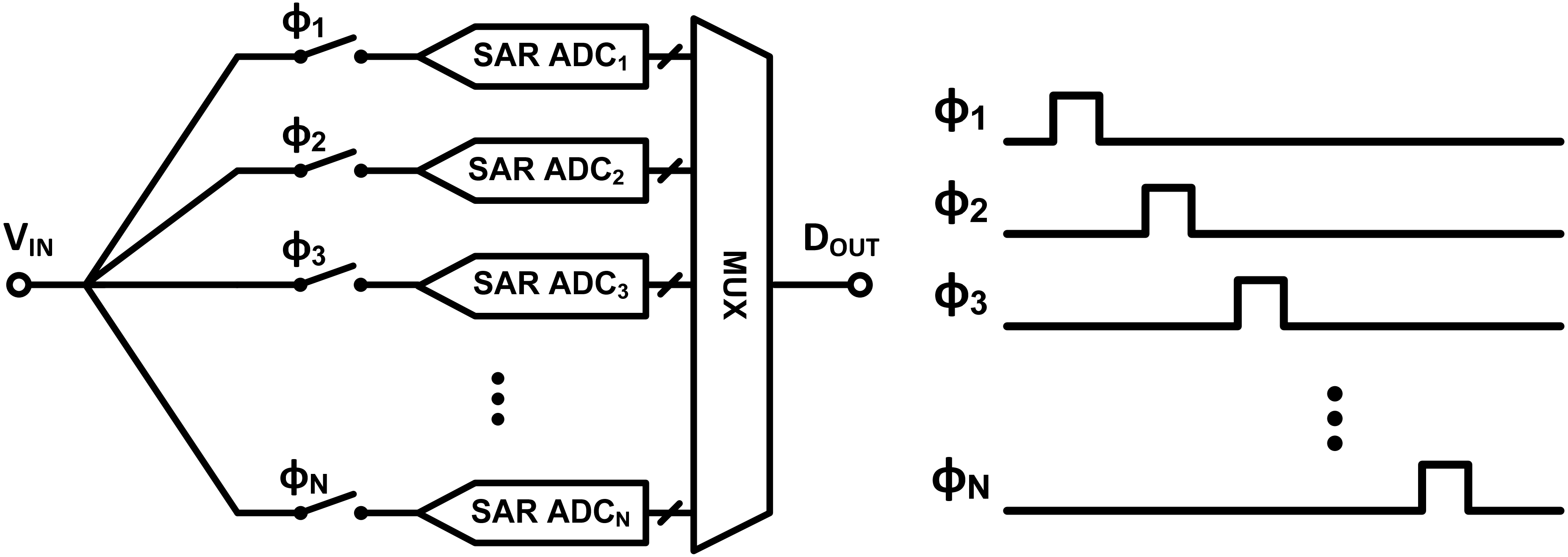
- **Motivation**
  - **Time-interleaved (TI) ADC**
  - **Timing skew and calibration**
- **Proposed TI SAR ADC**
  - **Block diagram**
  - **Circuit implementation**
  - **Timing skew estimation**
  - **Measurement result**
- **Conclusion**

Time-interleaved ADC



- **Time-interleaved (TI) SAR ADC**
  - Energy efficient solution to increase sampling rate
  - Effective sampling rate : $f_s = N \cdot f_{channel}$

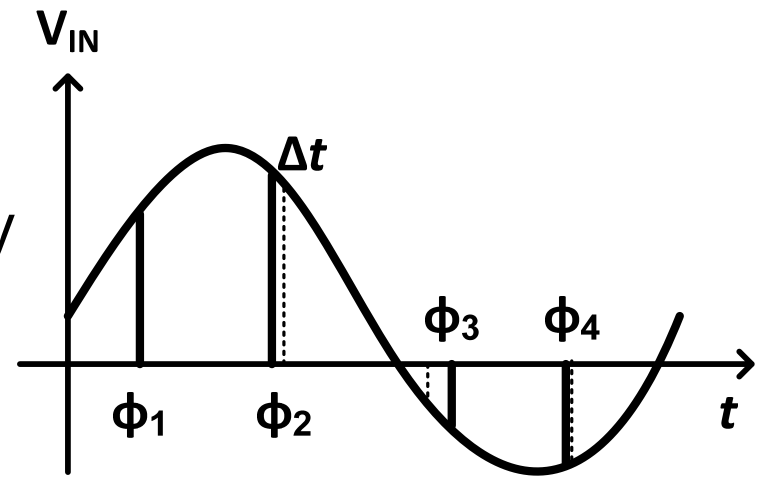
Time-interleaved ADC



- **Issues of TI ADC**
  - Offset mismatch
  - Gain mismatch
  - Timing skew

Timing Skew and Calibration

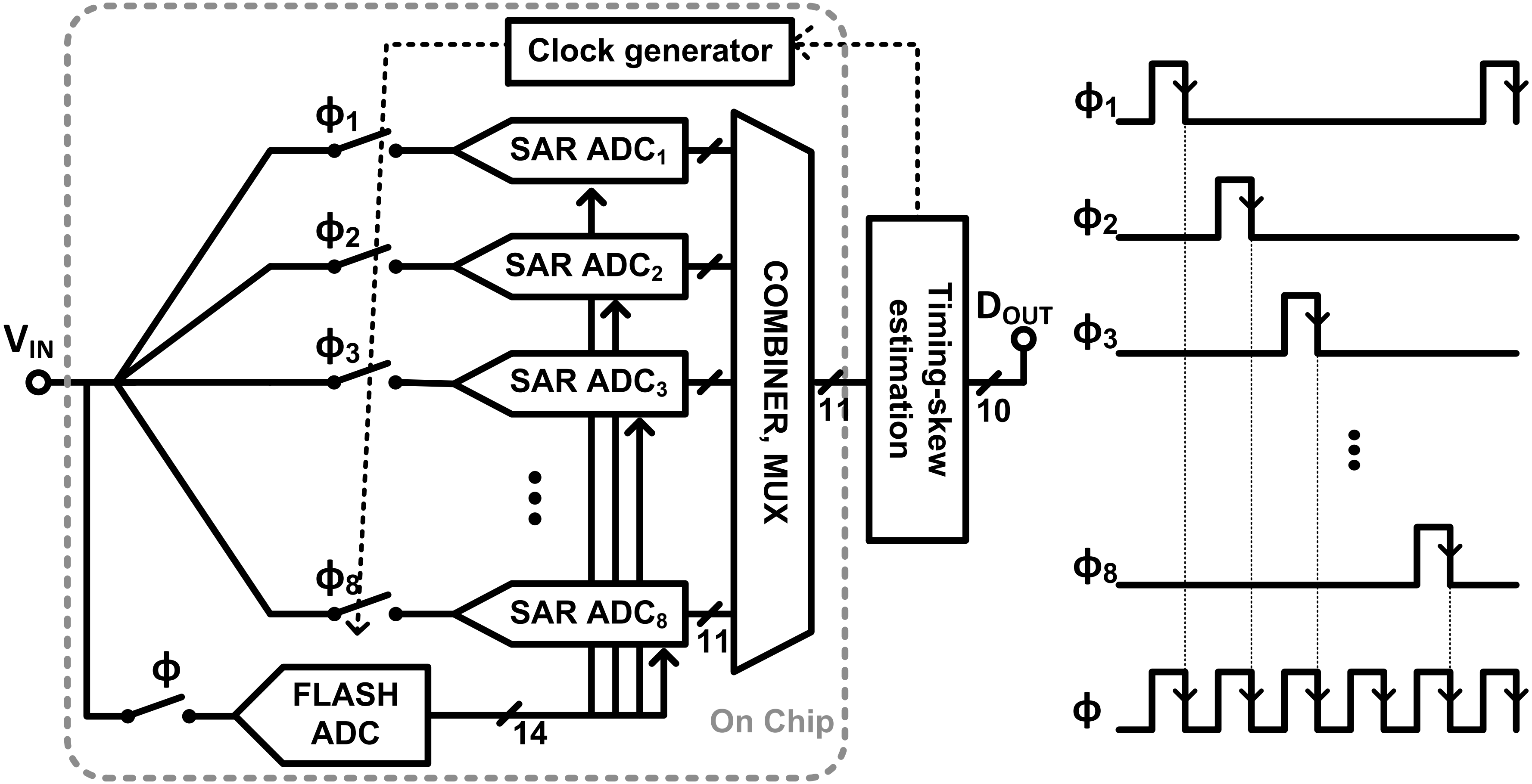
- **Timing skew error :** $\varepsilon = \frac{dV_{in}}{dt} \cdot \Delta t$
  - Proportional to the input frequency
  - Time-varying error



- **Timing skew calibration**
  - Timing skew estimation
    - Foreground : Predetermined input signal (linear ramp, sine wave)
    - Background : Additional channel as a reference in time

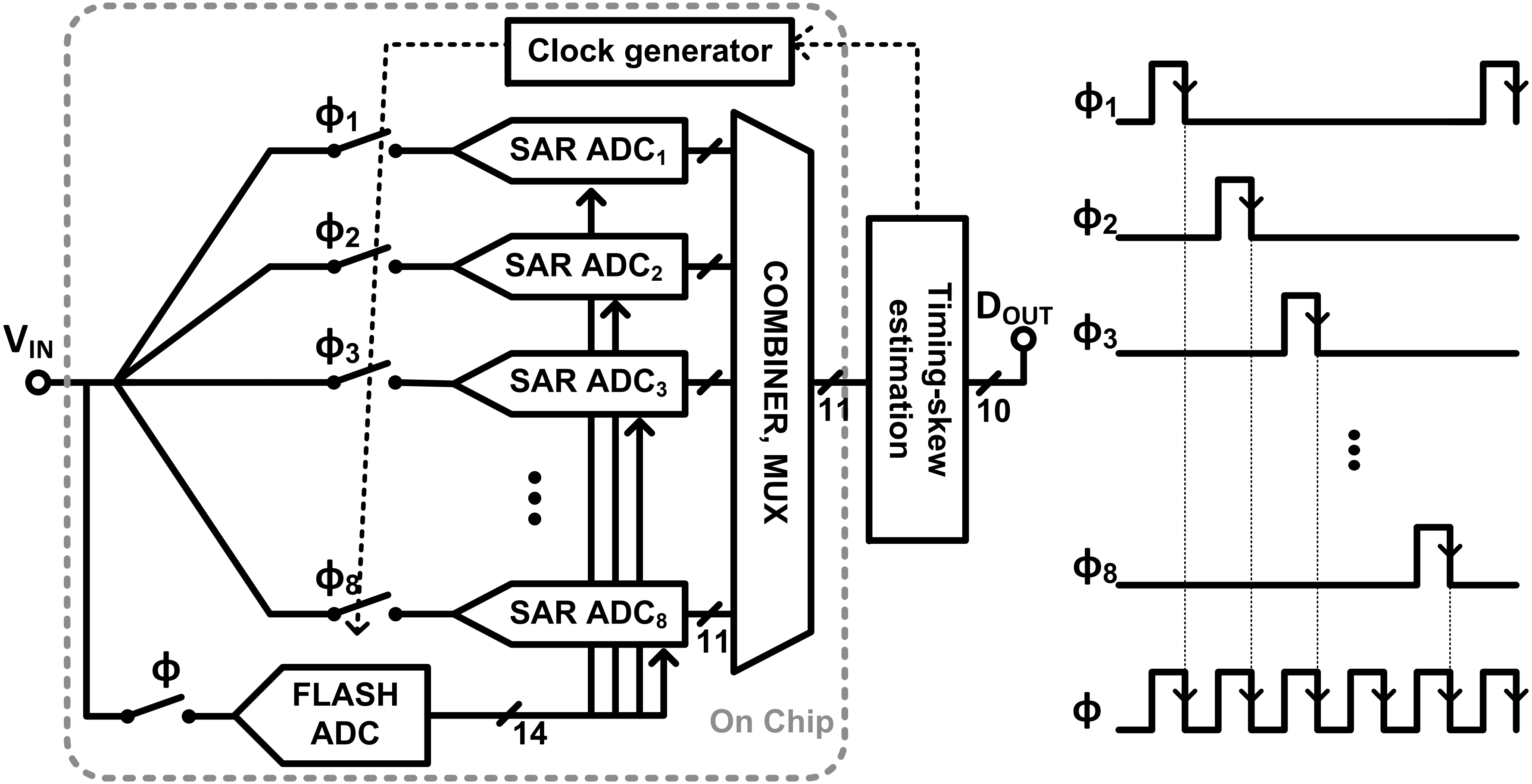
      [El-Chammas, JSSC 2011], [Stepanovic, JSSC 2013]
  - Timing skew correction
    - Digital approach : Fractional delay filters
    - Mixed signal approach : Variable delay for sampling clocks

Proposed 8-Way TI SAR ADC



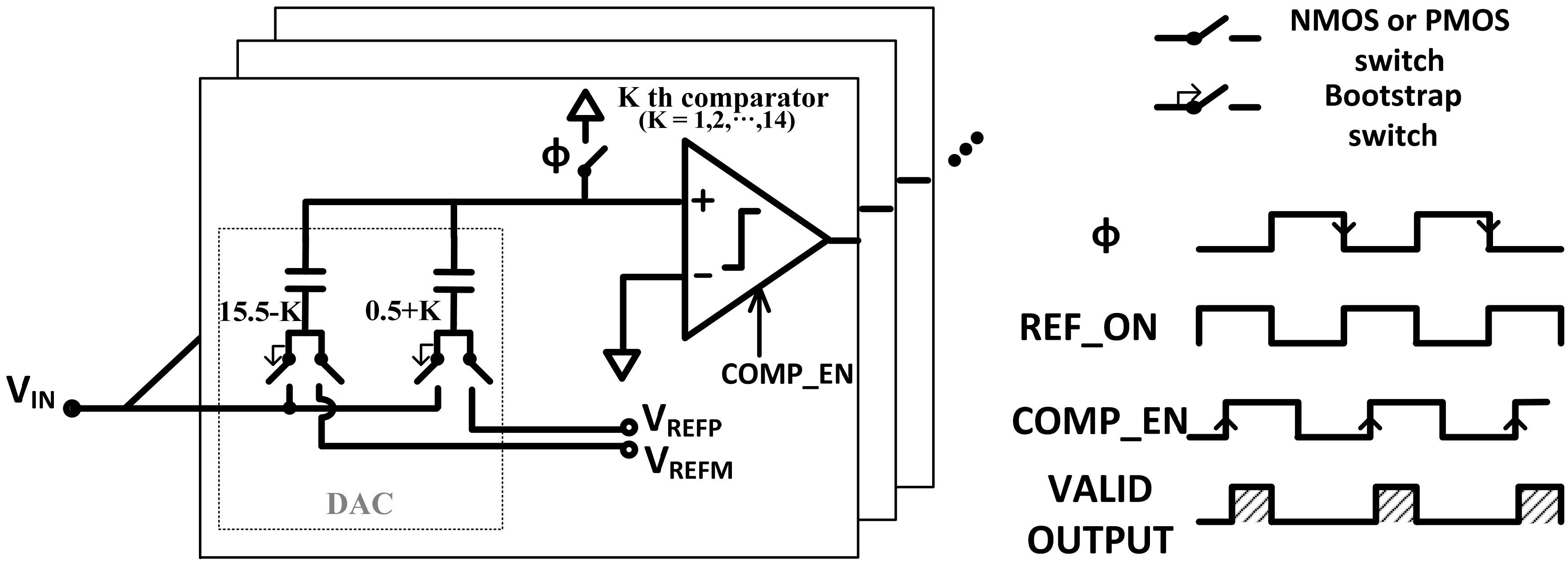
- **Flash ADC**
  - Resolve 4MSBs at $8 \cdot f_{channel}$ speed (ϕ)
  - Used as a reference in timing

Proposed 8-Way TI SAR ADC



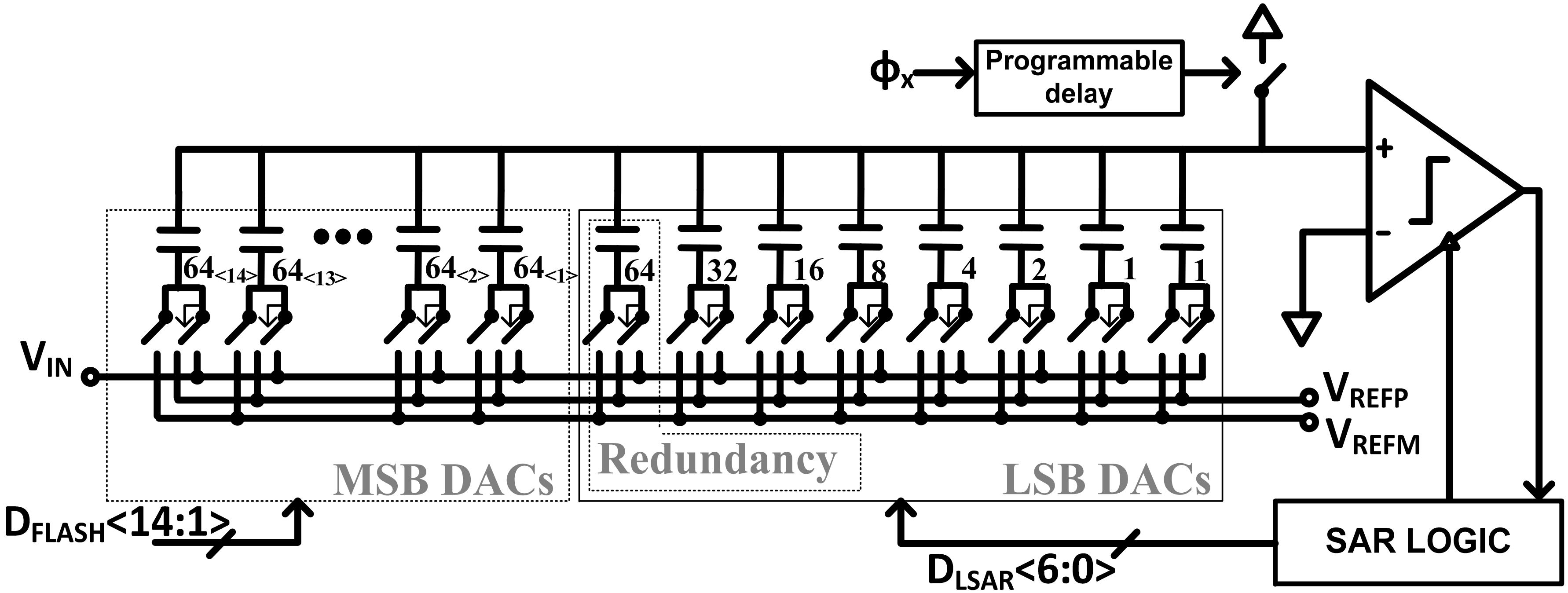
- **SAR ADCs**
  - Resolve 7LSBs at $f_{channel}$ speed (ϕ_X)
  - Align ϕ_X to ϕ

Flash ADC Implementation



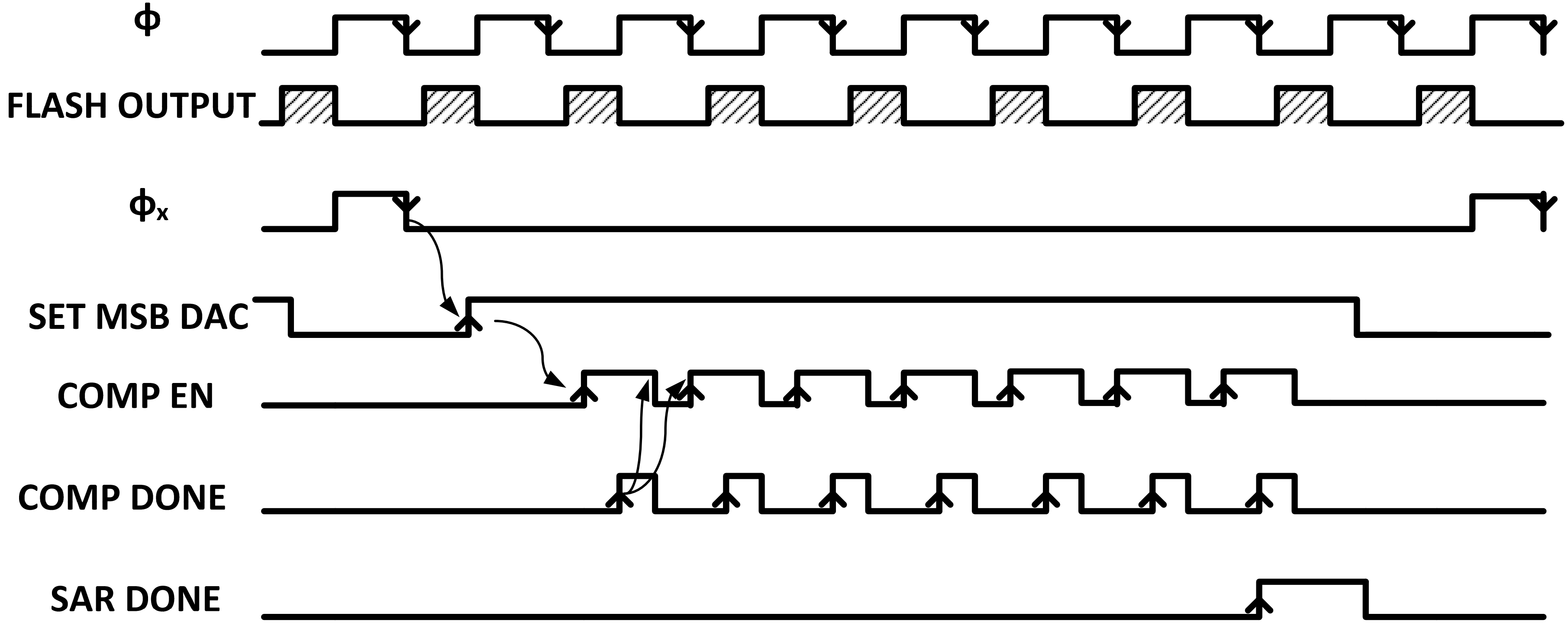
- **4 bit Flash ADC**
  - Rail-to-rail input
  - Fully differential structure
  - No static power consumption
  - Scaled version of SAR ADC for good timing match

SAR ADC Implementation



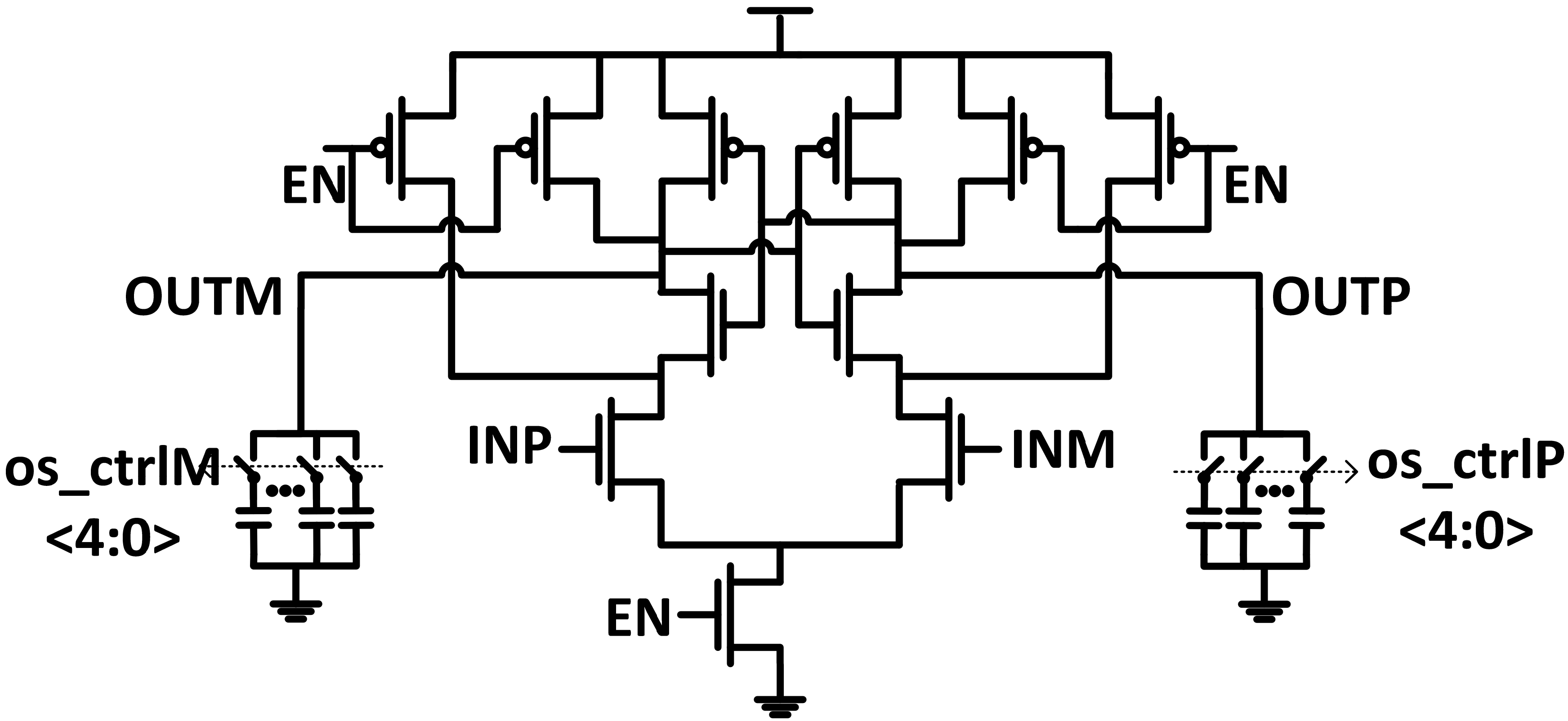
- **10 bit SAR ADC**
  - 7 bit SAR conversion with 1 bit redundancy
  - MSB DACs controlled by flash ADC outputs
  - Custom designed 1fF unit capacitance

SAR ADC Timing



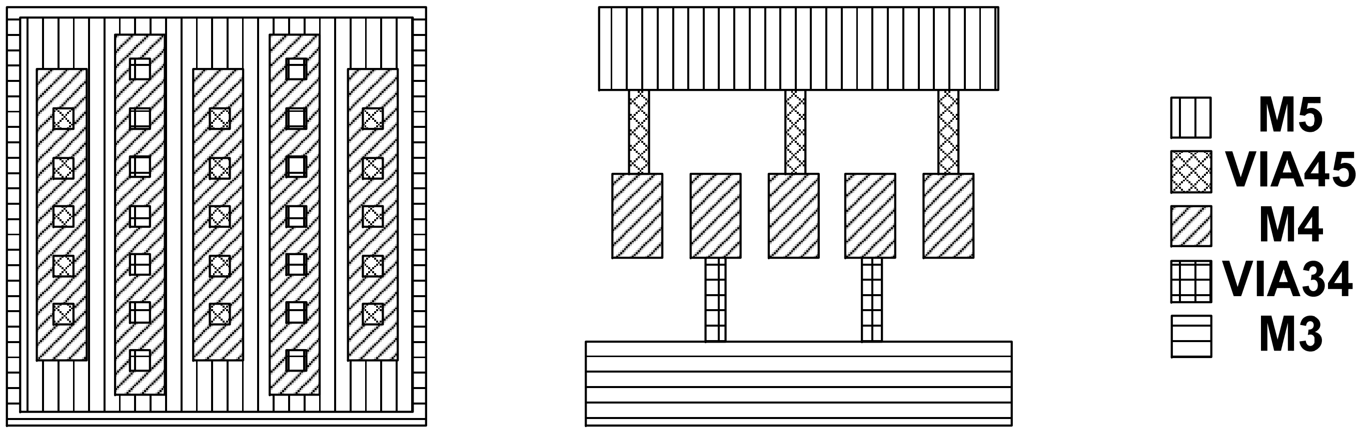
- **Asynchronous SAR logic**
  - Only 7 SAR cycles for 10 bit resolution

SAR Comparator



- Dynamic latch
- Offset control capacitor bank

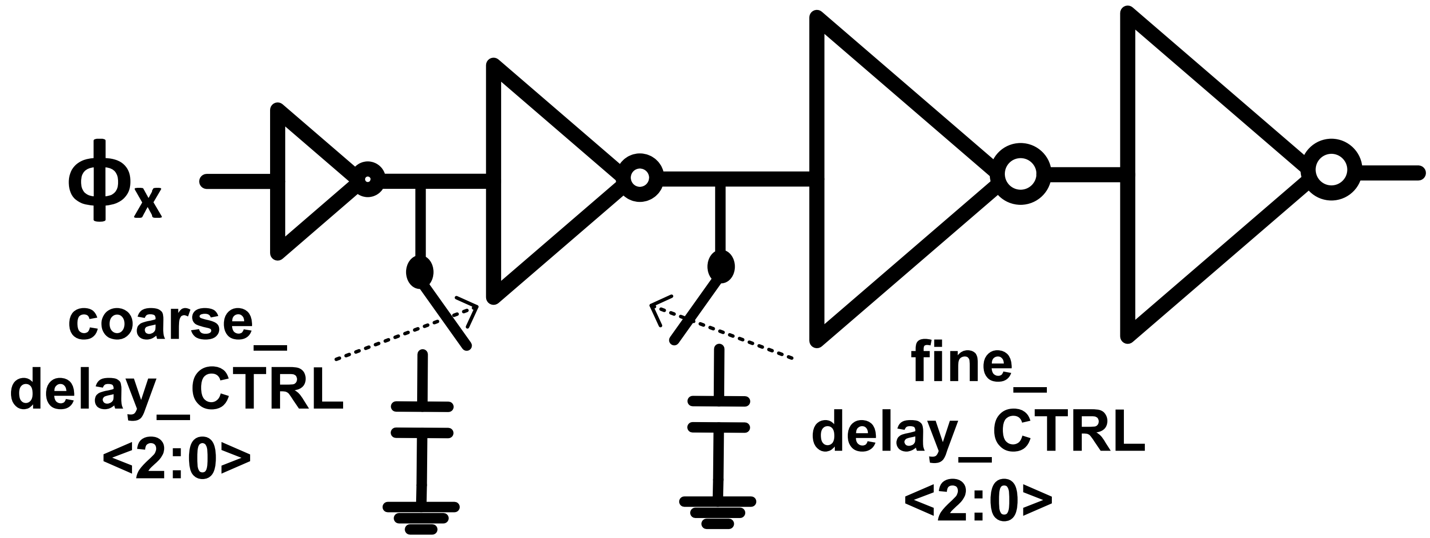
MIM/MOM Custom Capacitor



Top view　　Side view

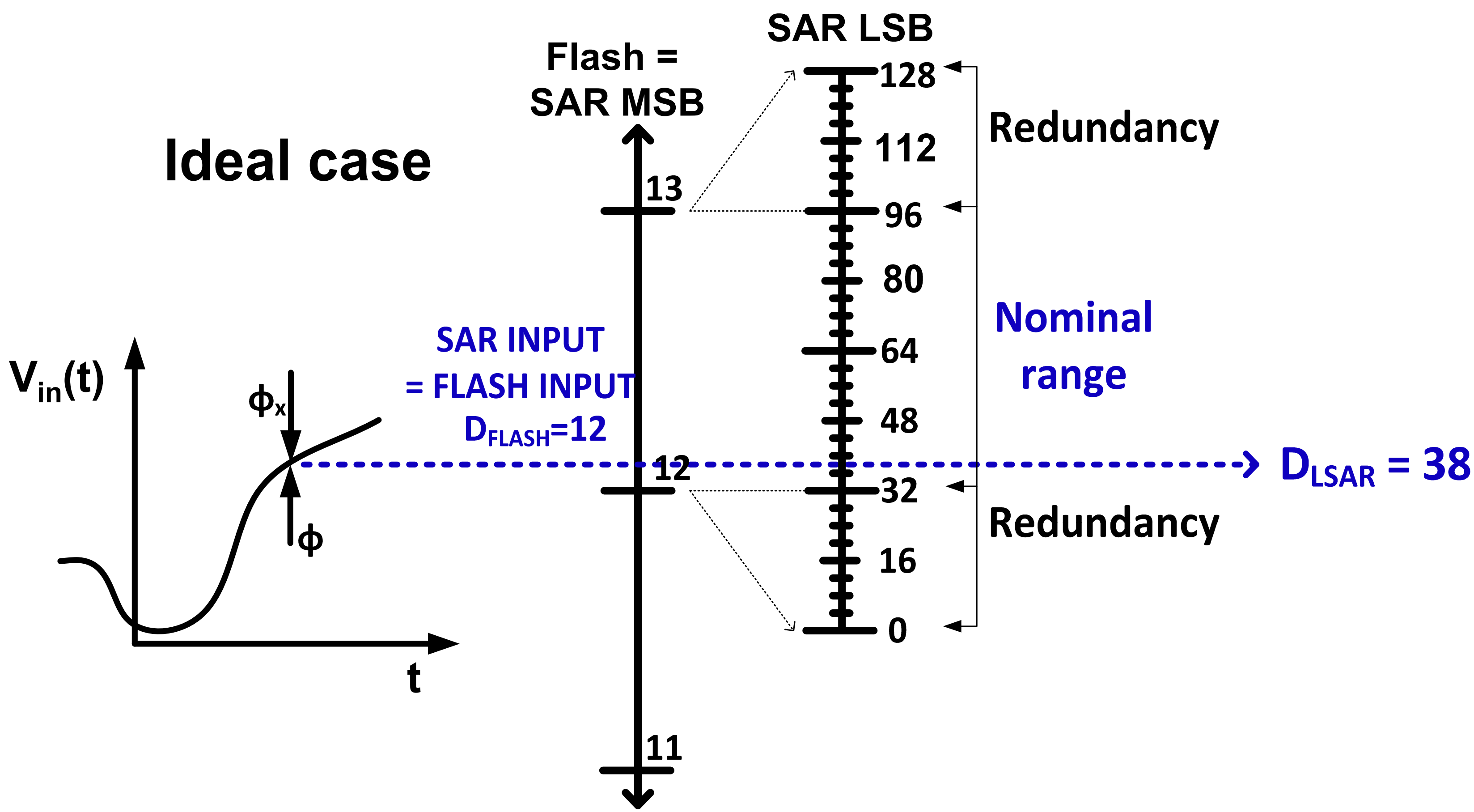
- **MIM structure**
  - Easy access to the elements in the capacitor array
  - Smaller parasitic cap on M5 (bottom plate)
- **MOM structure**
  - Higher density

Programmable Delay



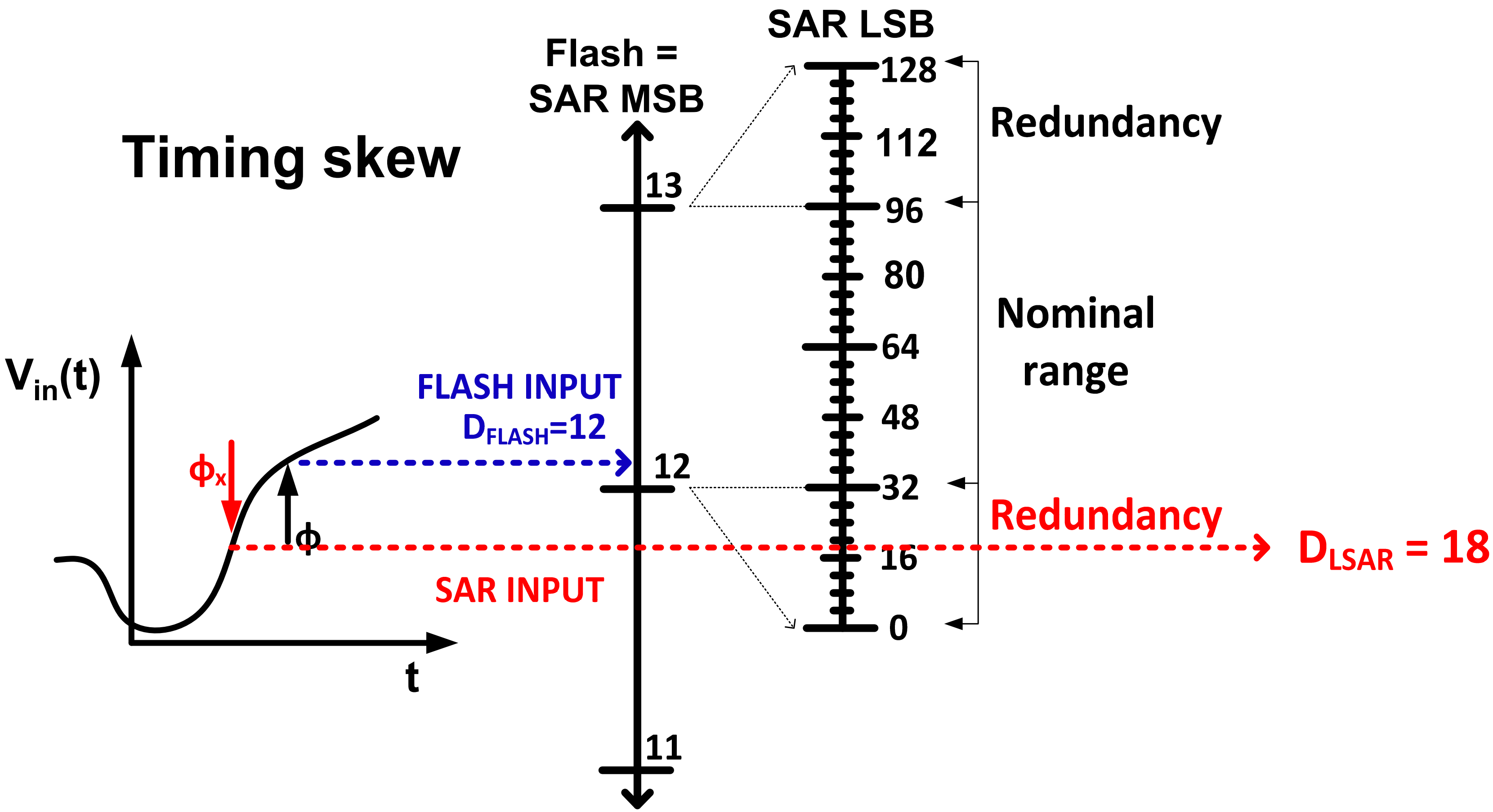
- Binary weighted capacitors at clock buffer
- Coarse(~2ps/code) and fine(~0.8ps/code) delay

Timing Skew Estimation



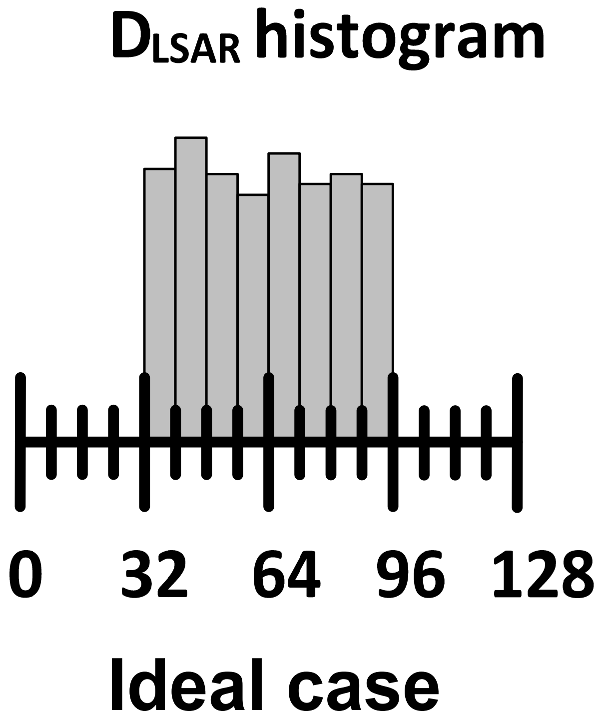
- If the flash and SAR samples are identical (**no timing skew**), the SAR output (D_{LSAR}) is in **nominal range**

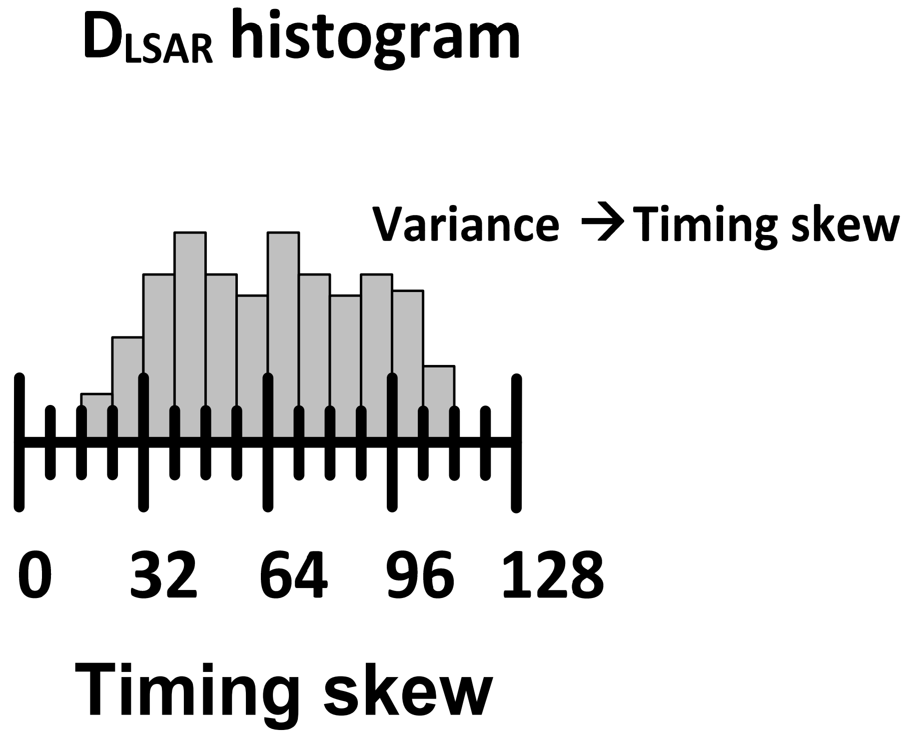
Timing Skew Estimation



- If the flash and SAR samples are different (**timing skew**), the SAR output (D_{LSAR}) is in the **correction range**

Timing Skew Estimation

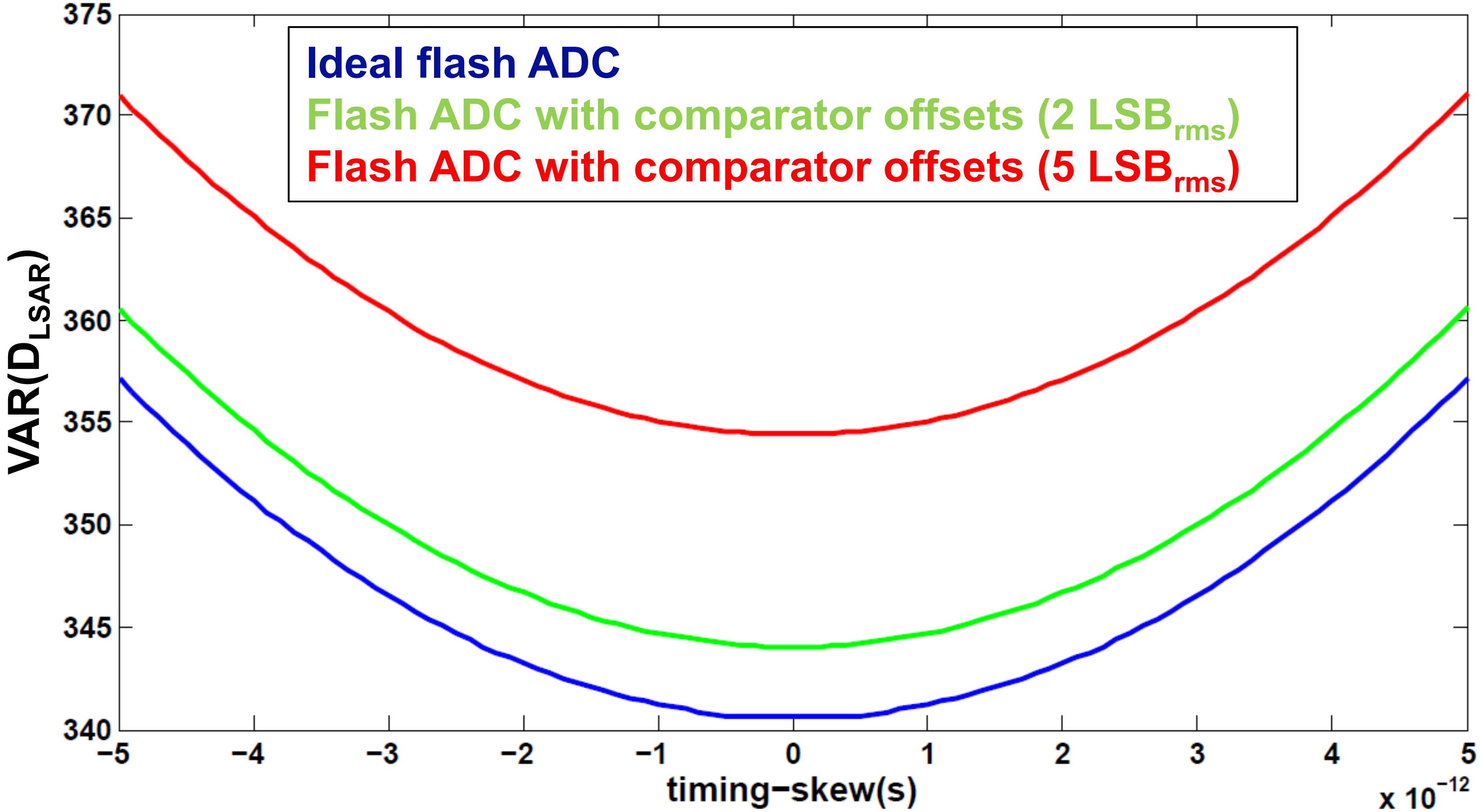




- SAR sampling clocks (ϕ_x) are aligned to flash sampling clock (ϕ) when VAR(D_{LSAR}) is minimum

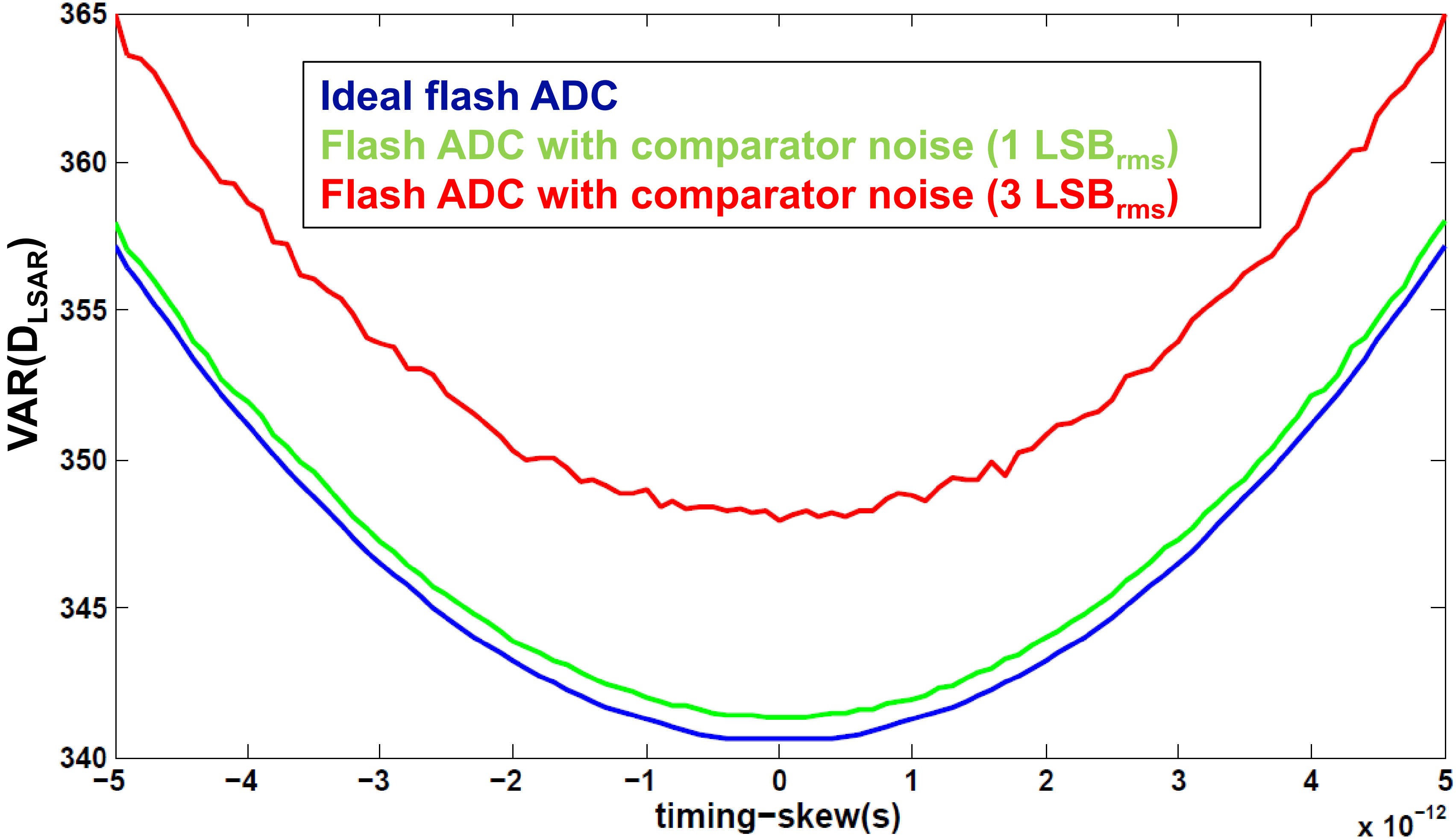
Behavioral Simulation

- Comparator offsets of the flash ADC



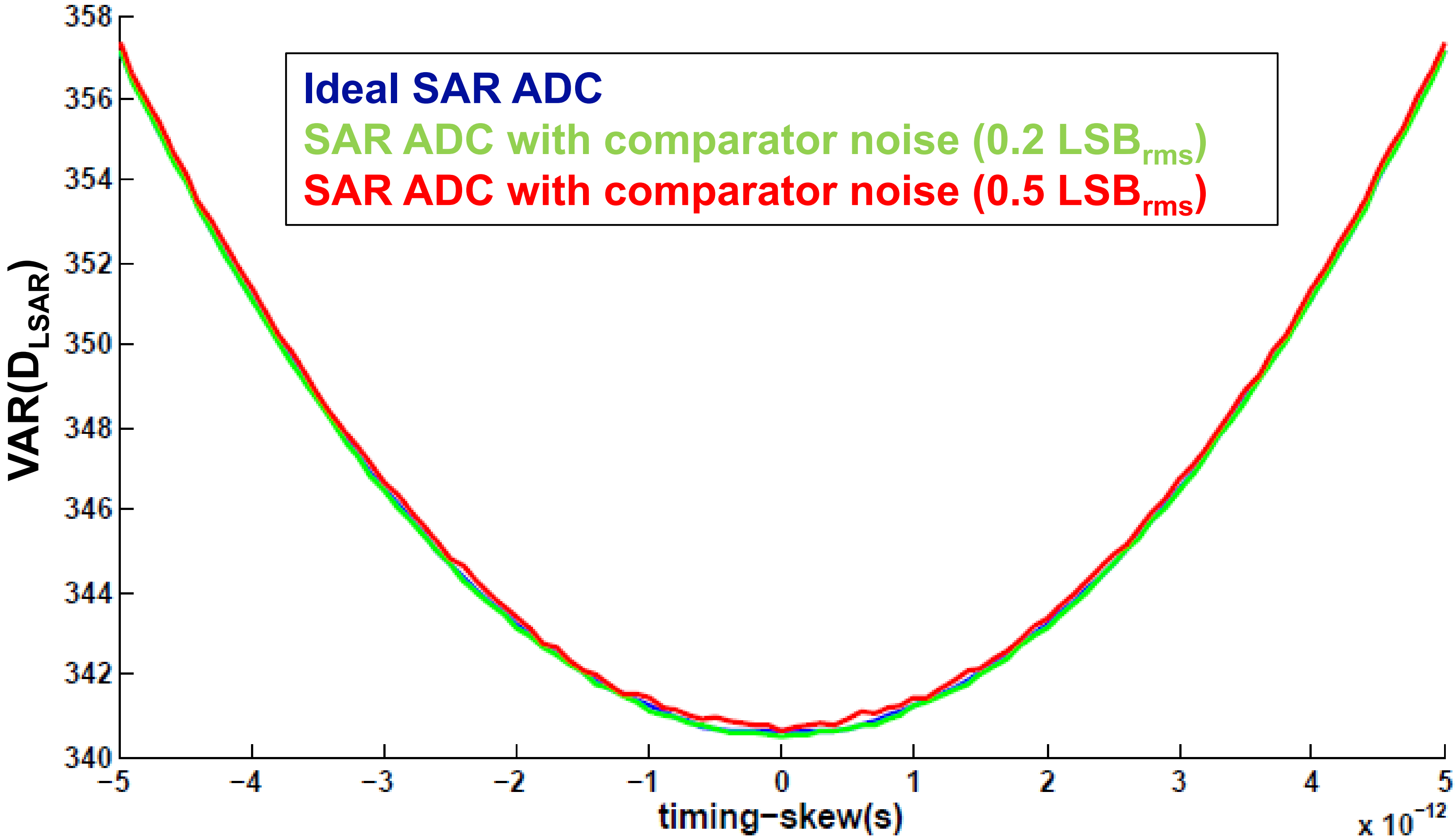
Behavioral Simulation

- Comparator noise of the flash ADC



Behavioral Simulation

- Comparator noise of the SAR ADC



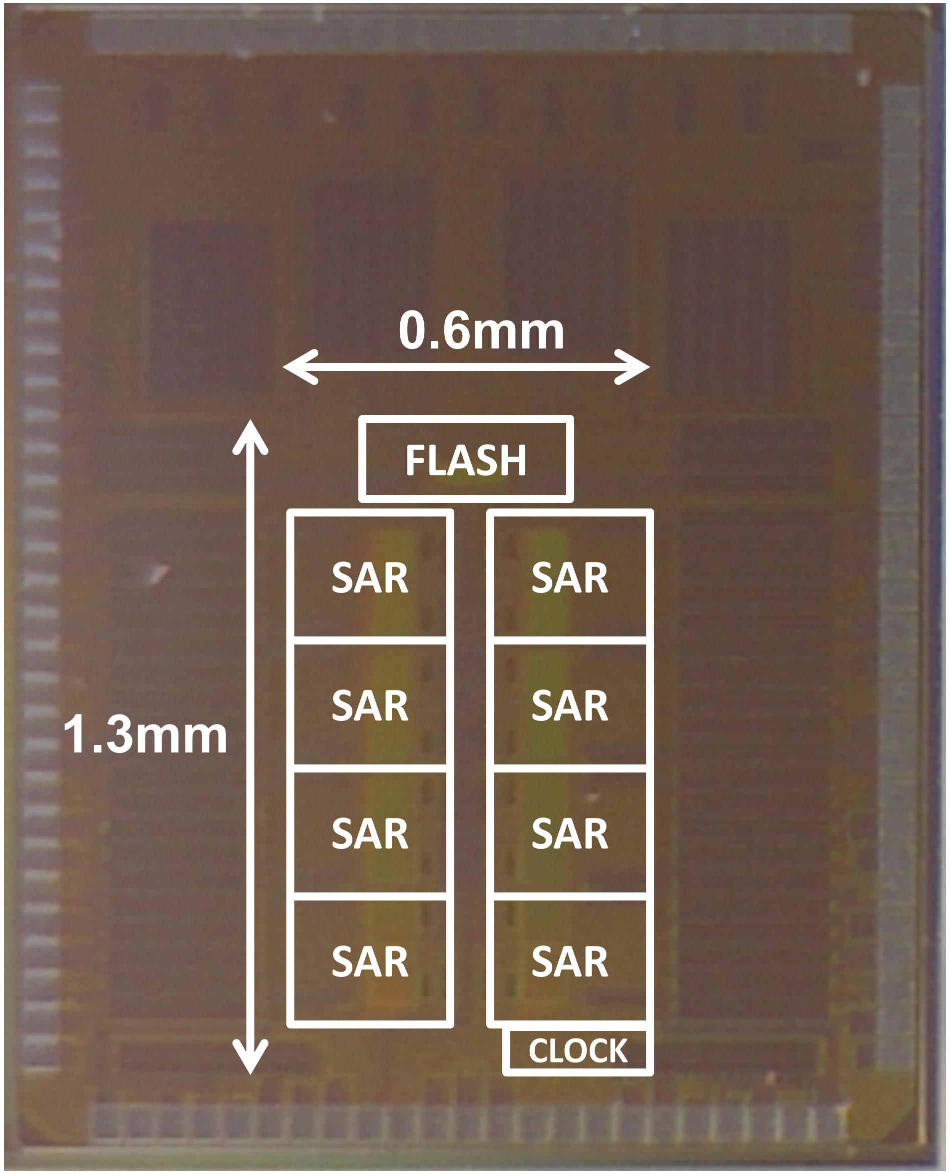
Advantages

- **Smaller chip area**
  - Proposed : 1 flash and 8 SAR ADCs ➔ 0.45mm^2
  - Conventional : 11 SAR ADCs ➔ 0.58mm^2 (estimated)
- **Reduced ADC reference power**
  - Proposed : 1.3 mW
  - Conventional : 2.3 mW (estimated)
- **Timing skew estimation can be applied to other ADCs (e.g. TI pipeline ADCs)**

Limitations

- **The ADC requires a flash ADC which runs at full speed**
  - **Speed improves with technology scaling**
- **Input signal must remain busy during calibration**

Die Photo



TSMC 65nm

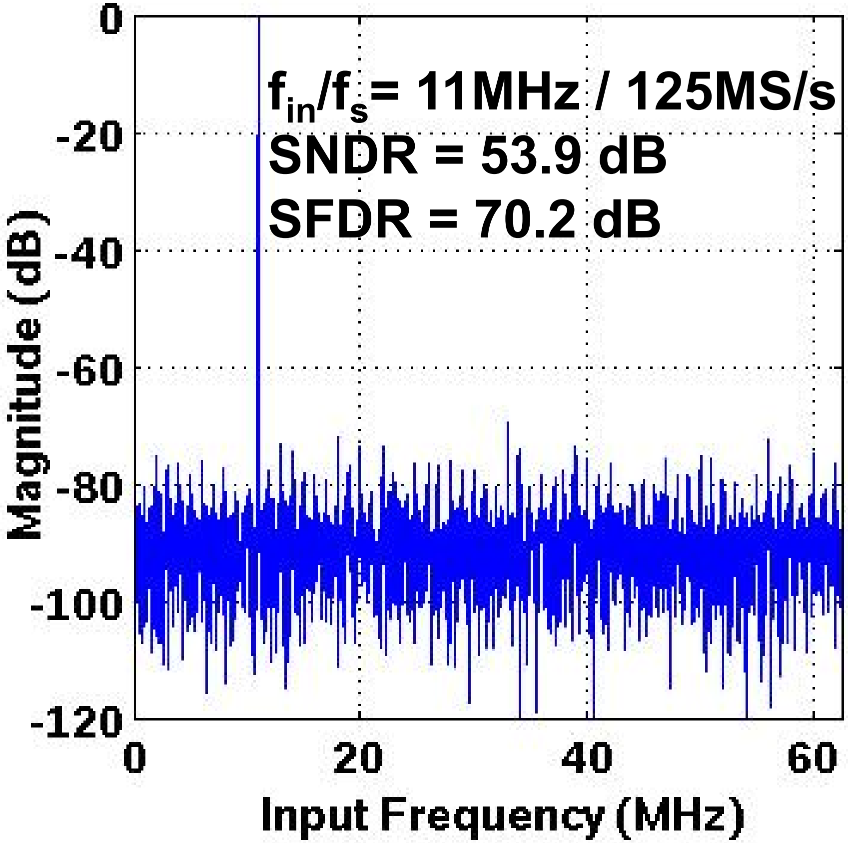
ADC core size :

0.6 mm X 1.3 mm

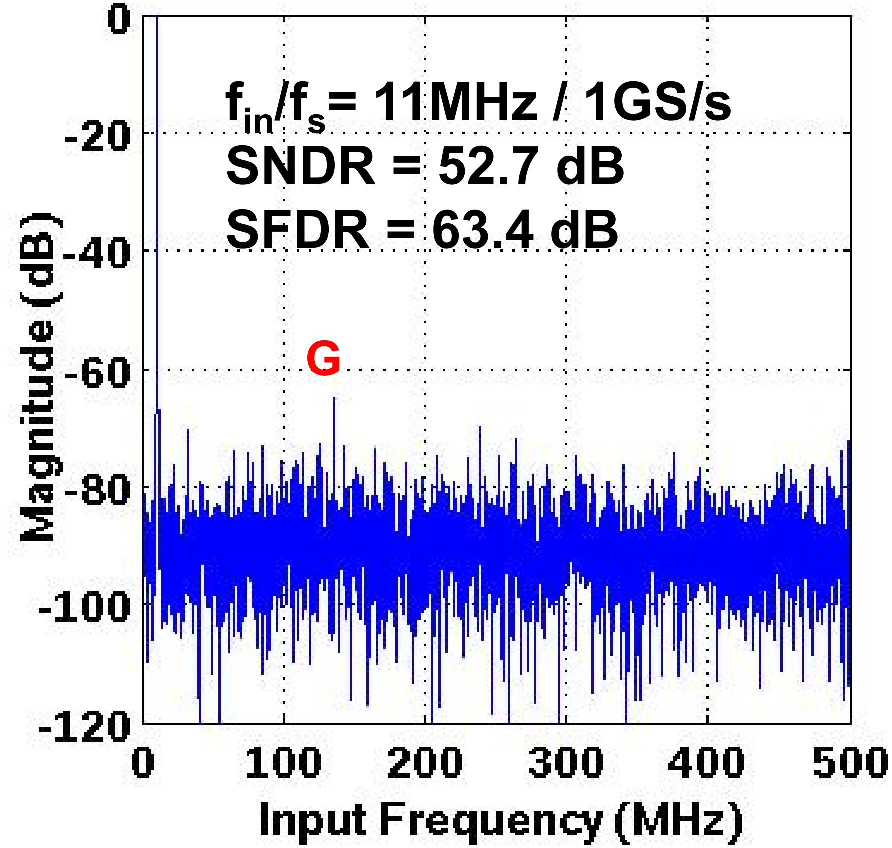
Measurement Results

- Before Calibration : Low frequency input

One channel



8 channel TI

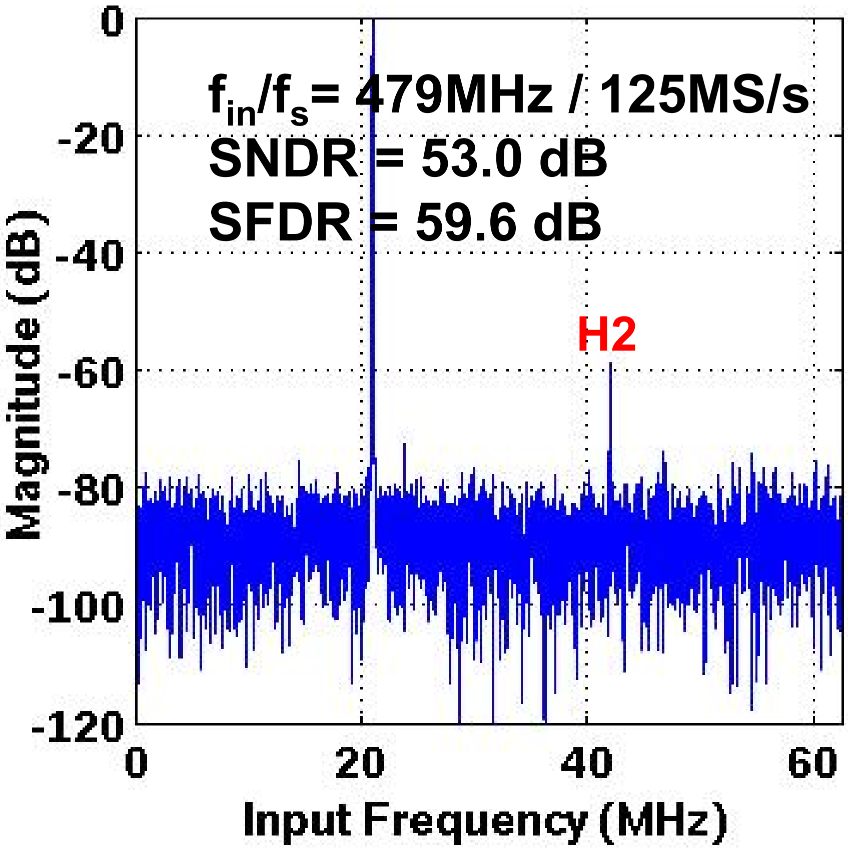


G : gain mismatch

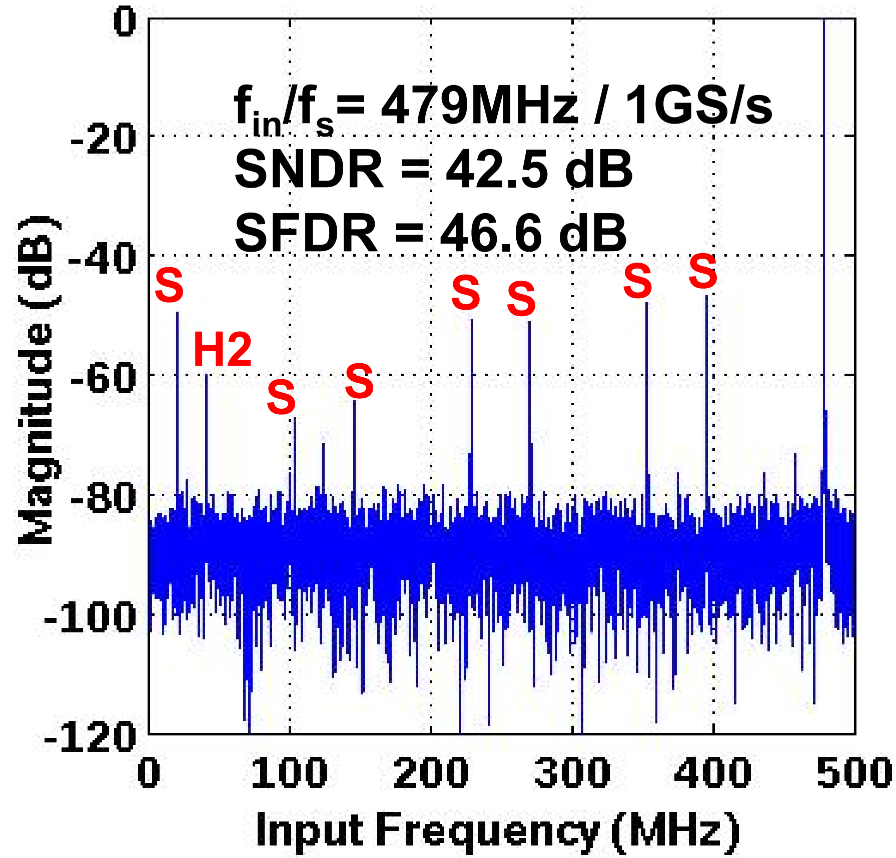
Measurement Results

- **Before Calibration : High frequency input**

One channel



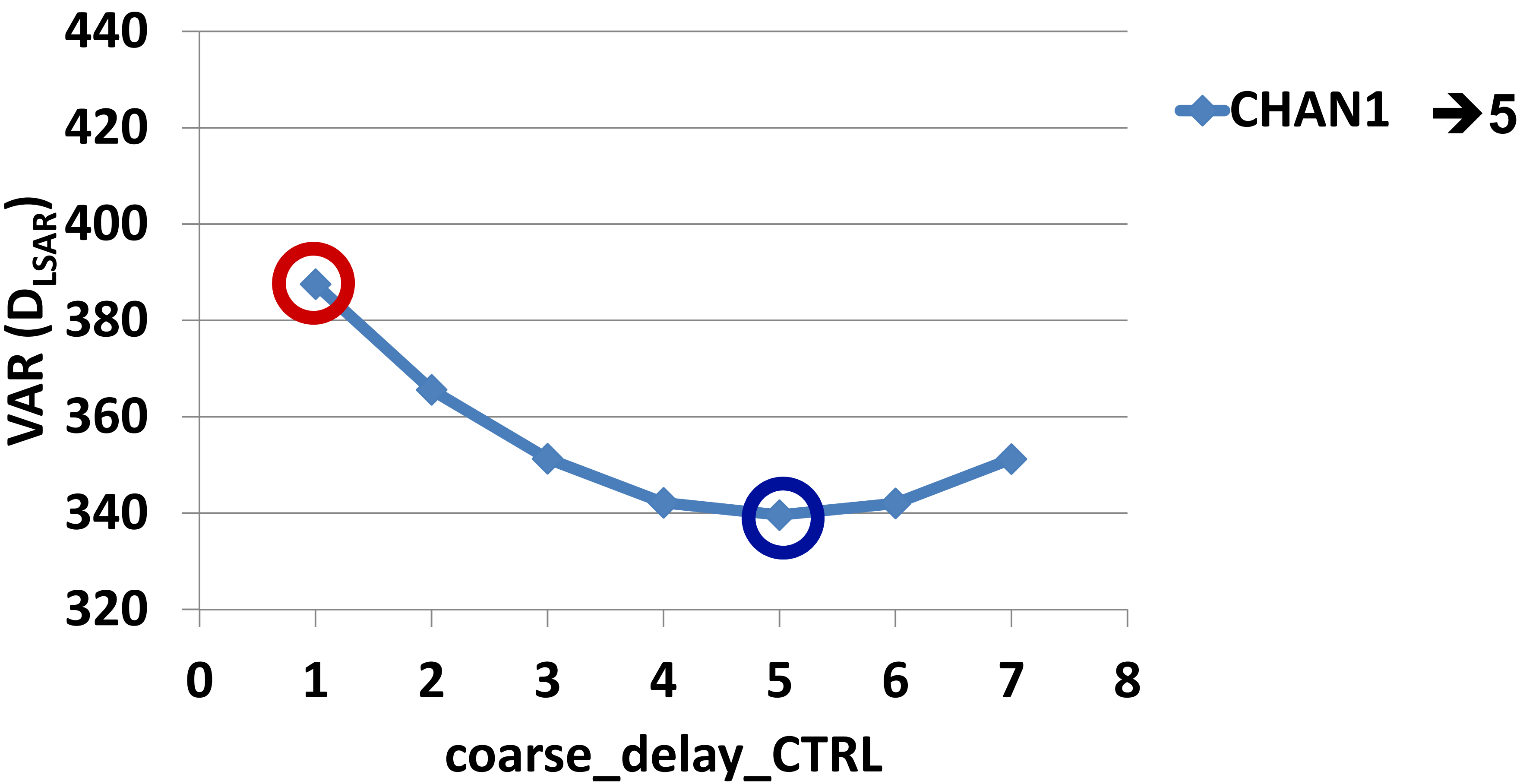
8 channel TI



H : harmonic
S : timing skew

Measurement Results

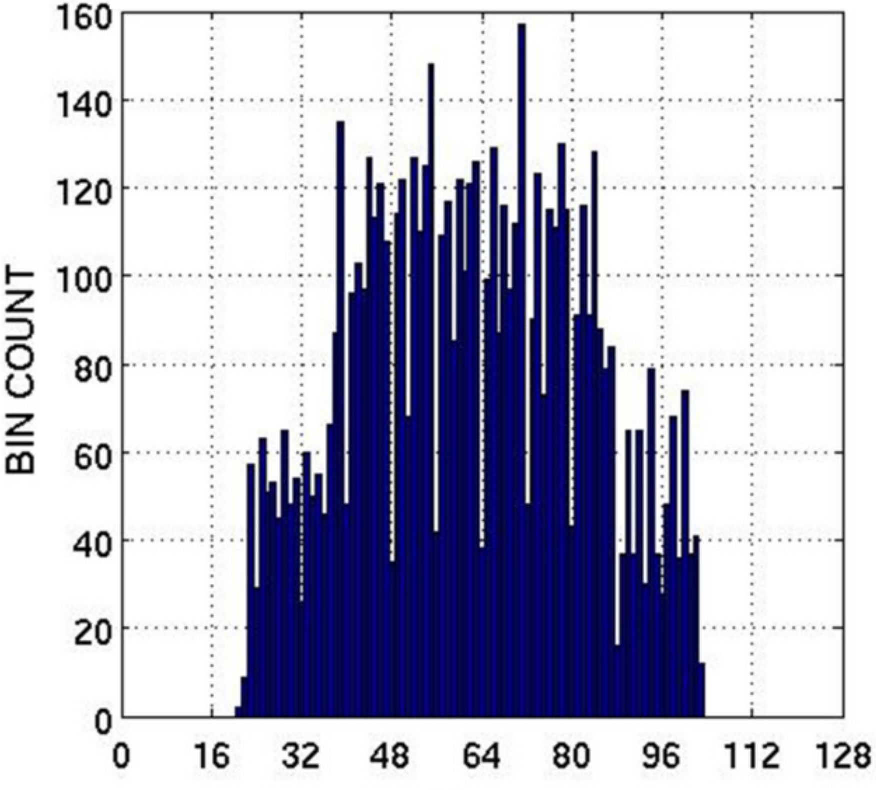
- **Calibration Process : VAR (D_{LSAR})**



Measurement Results

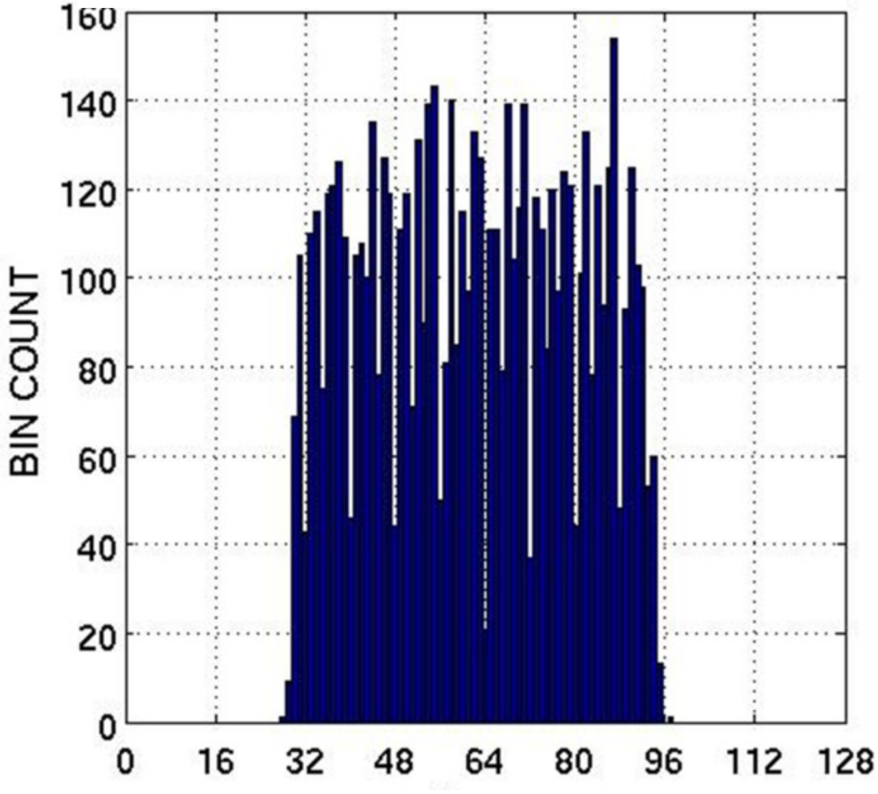
- Calibration Process : D_{LSAR} histogram

coarse_delay_CTRL=1



D_{LSAR} (D_{FLASH} =7)

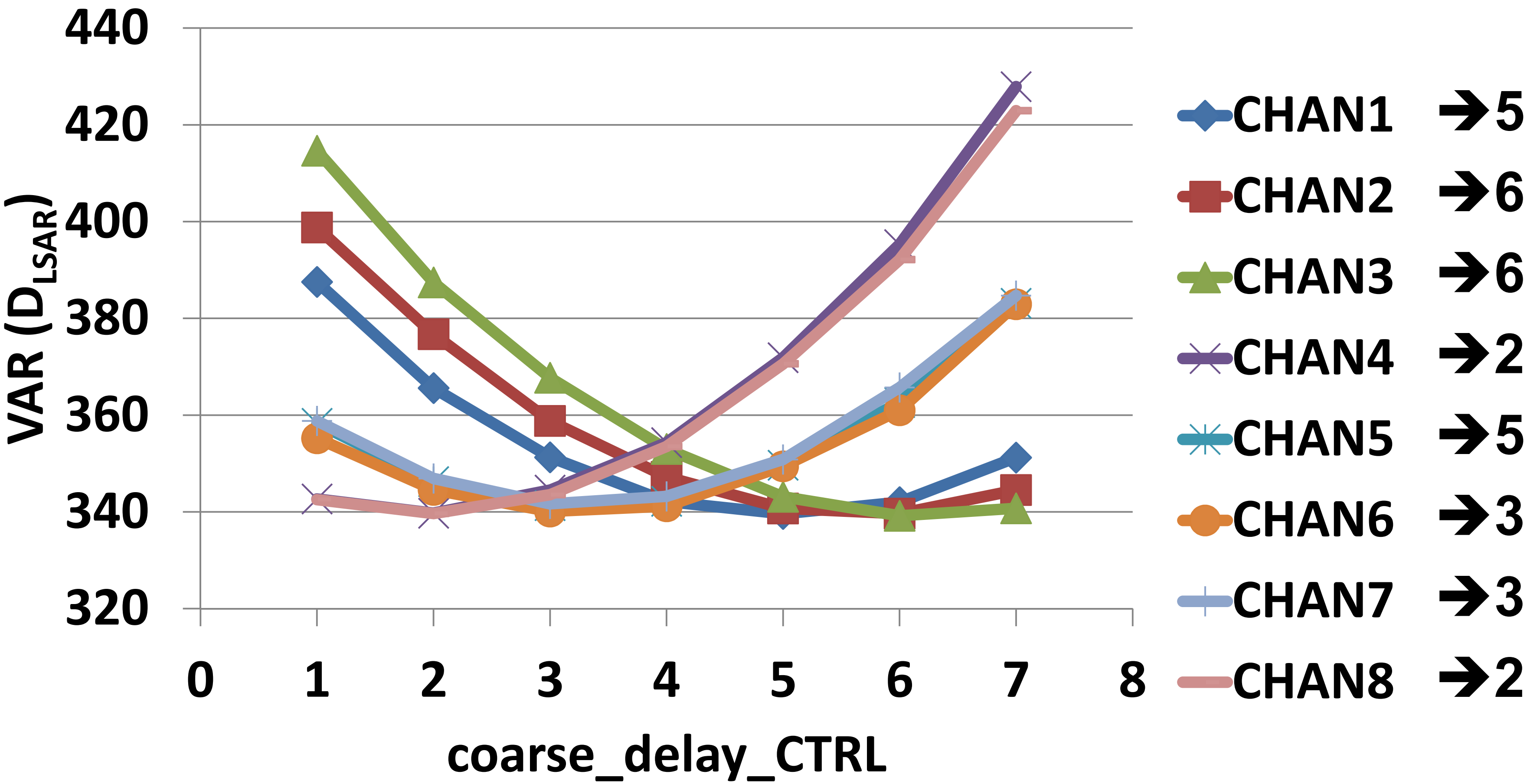
coarse_delay_CTRL=5



D_{LSAR} (D_{FLASH} =7)

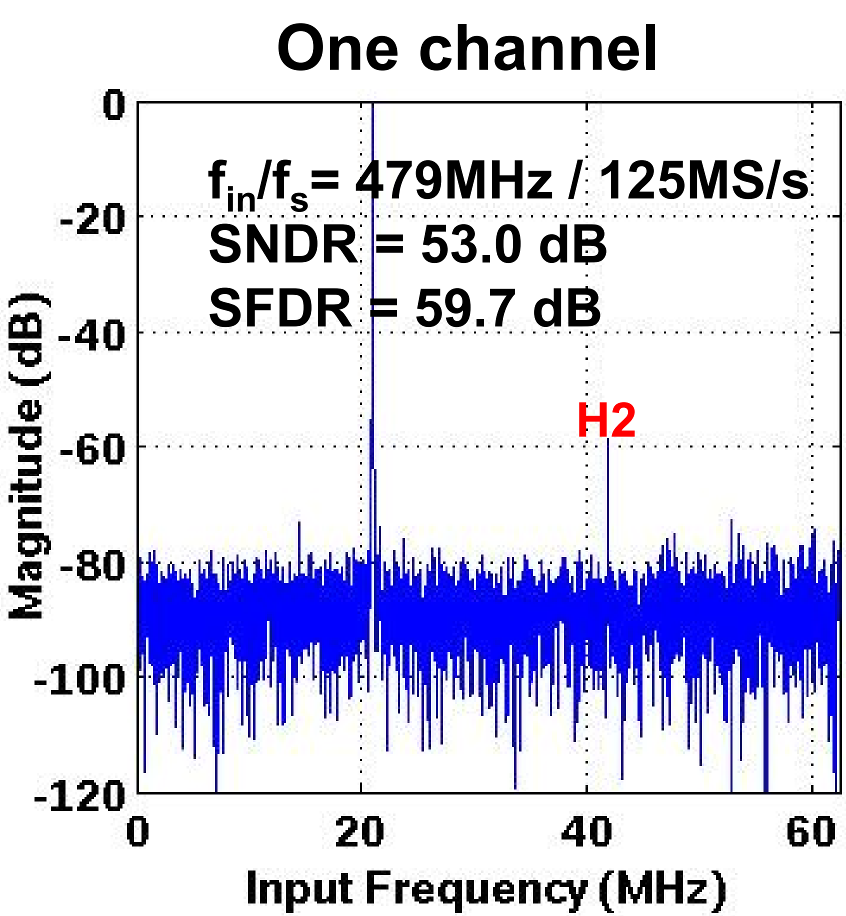
Measurement Results

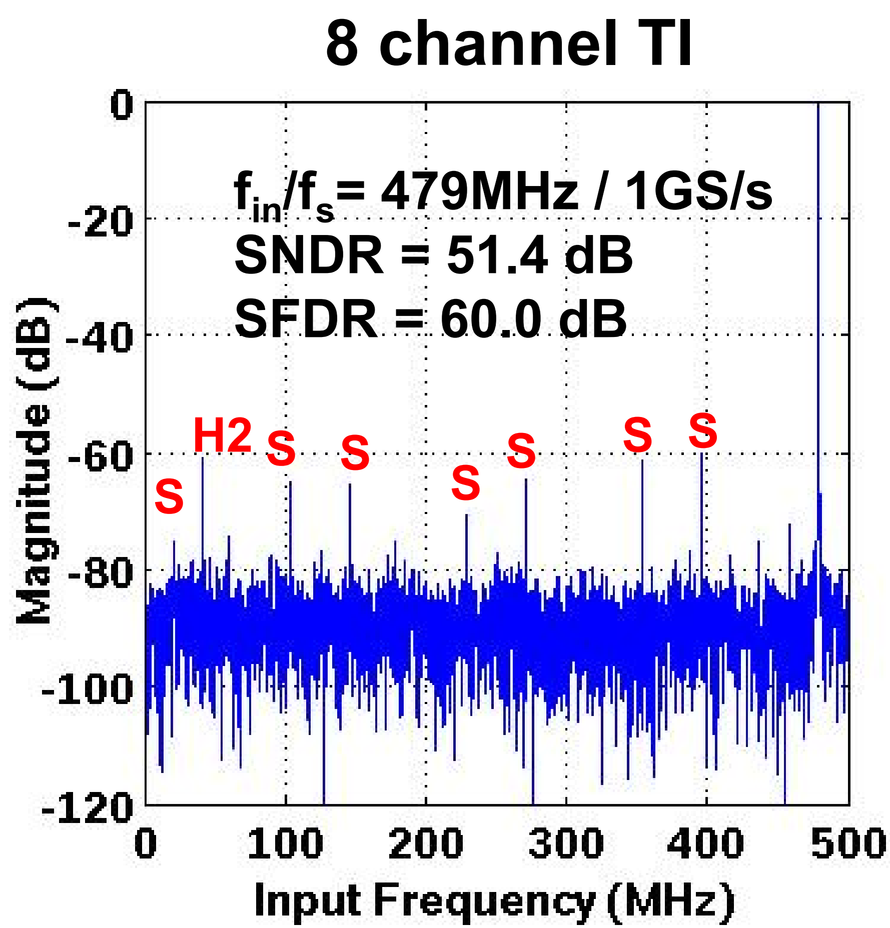
- **Calibration Process : VAR (D_{LSAR})**



Measurement Results

- **After Calibration : High frequency input**

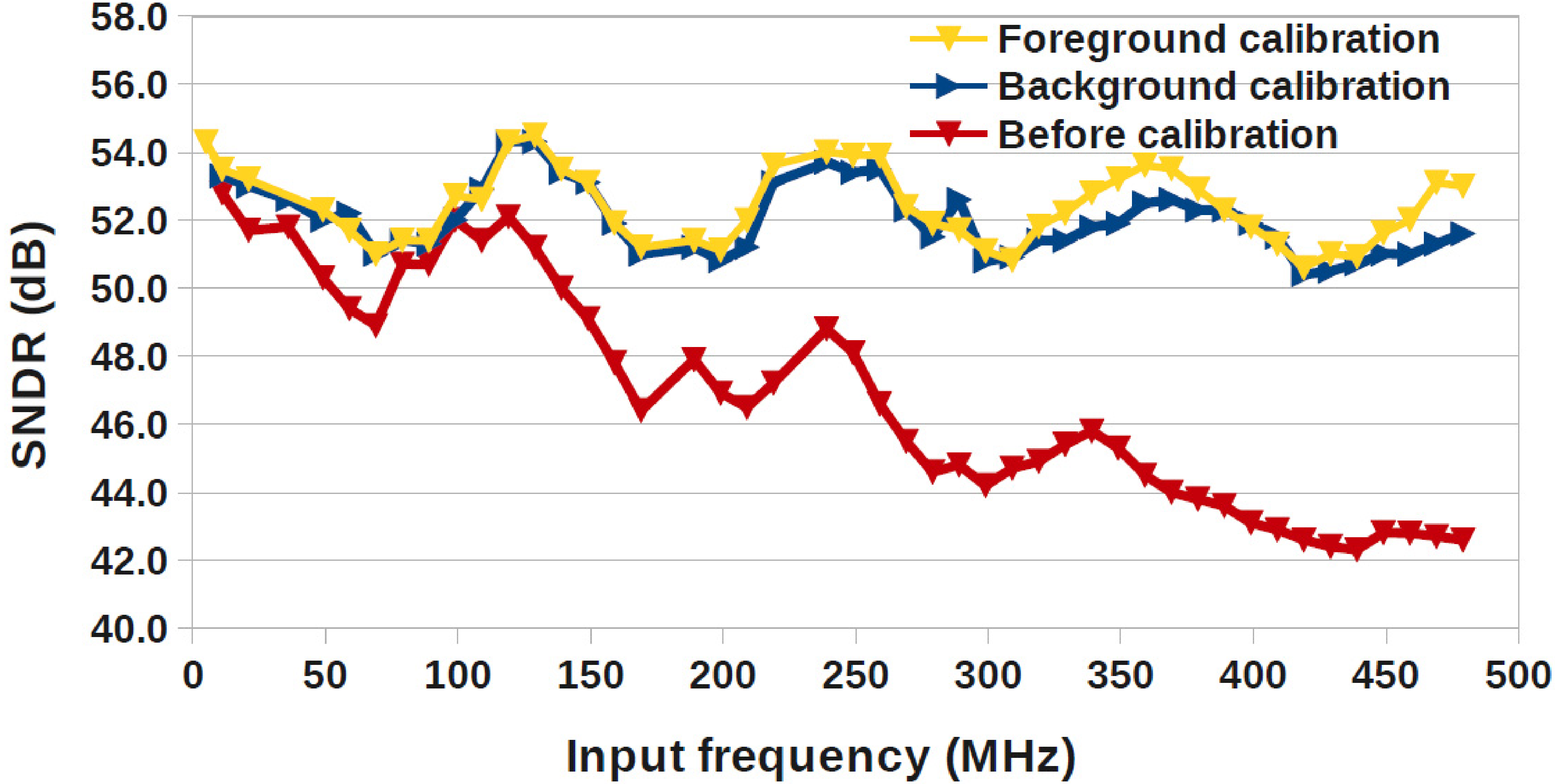




H : harmonic
S : timing skew

Measurement Results

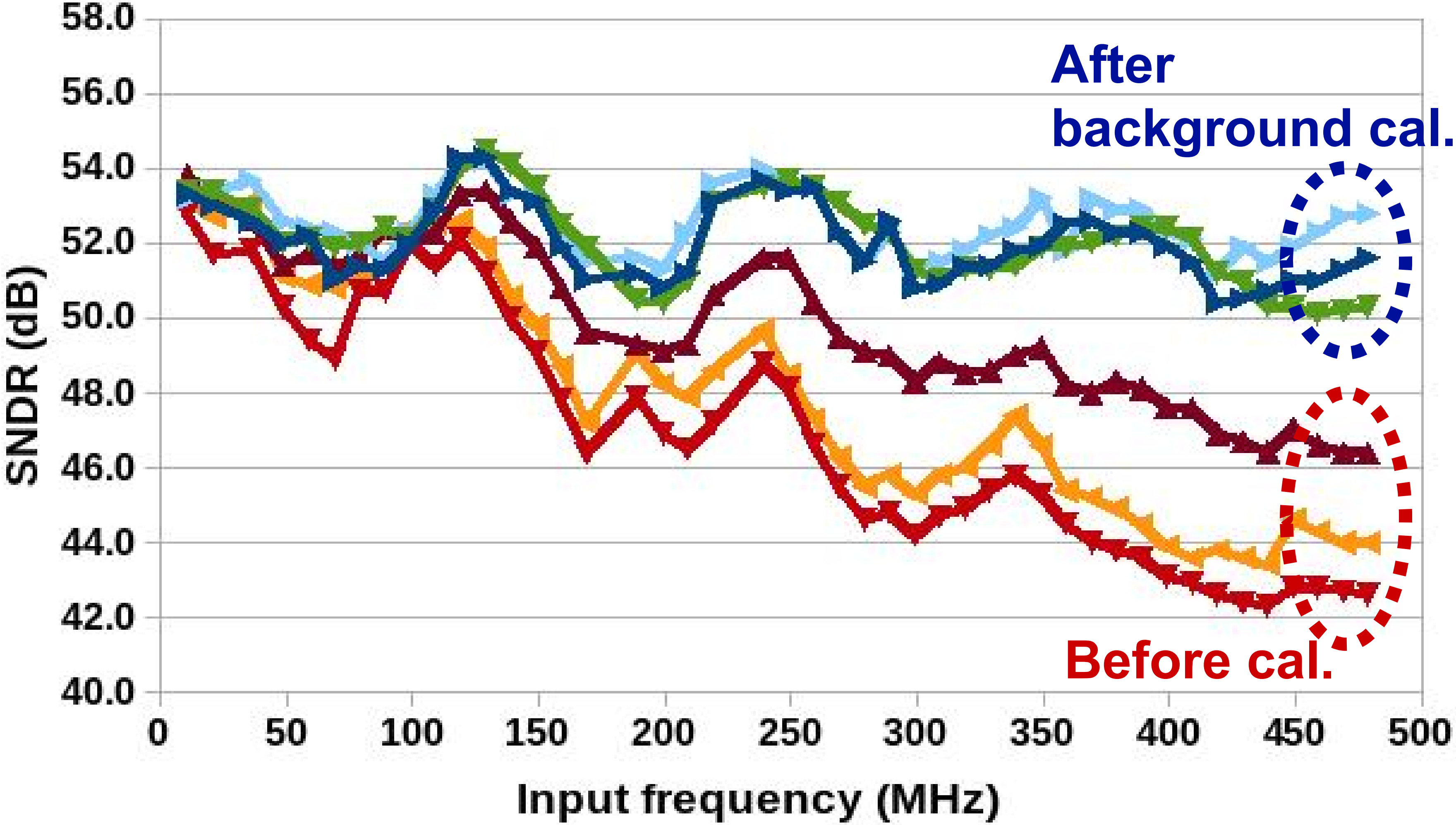
- SNDR vs. f_{in}



- Note: the SNR waviness is believed to be caused by data-dependent disturbances on the external input network

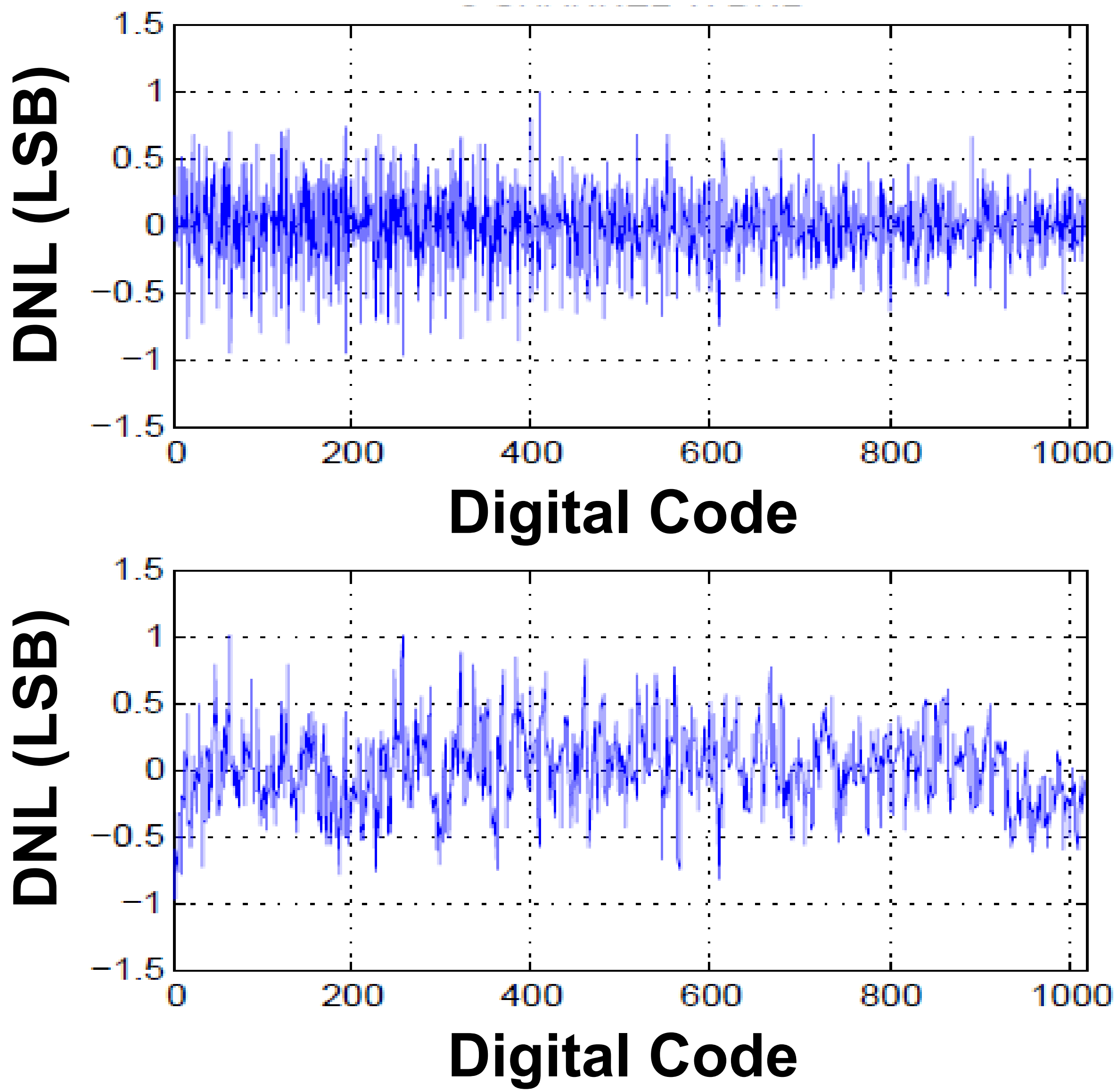
Measurement Results

- SNDR vs. f_{in} : 3 chips



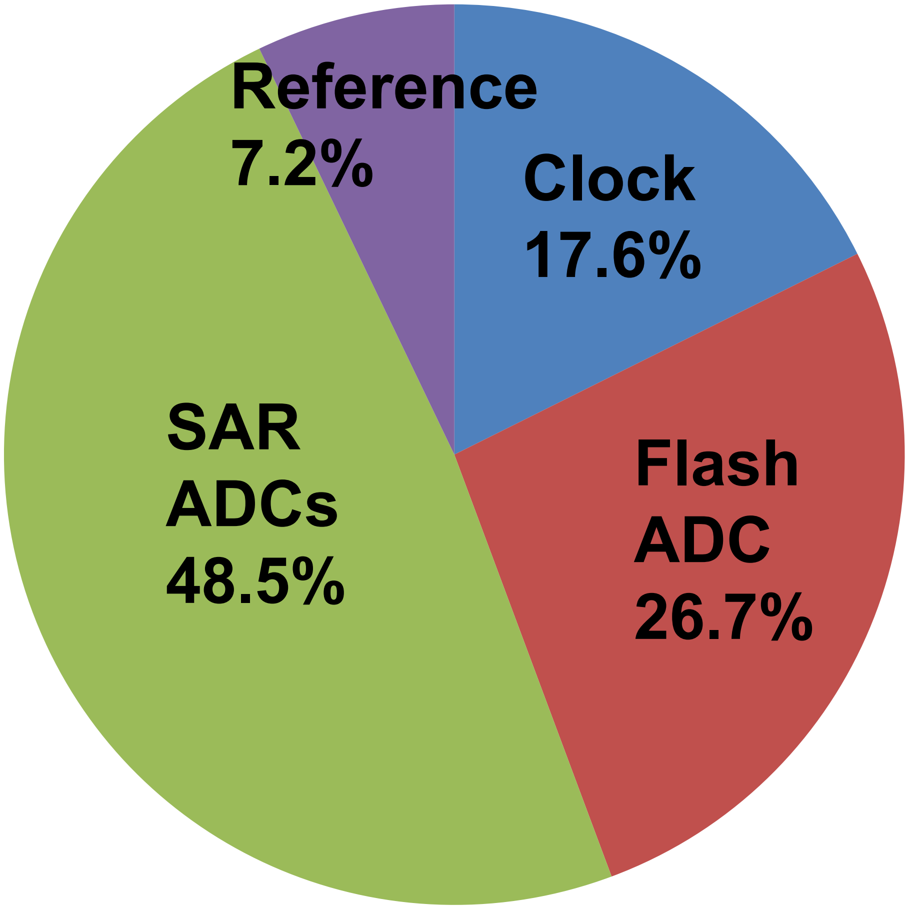
Measurement Results

- **DNL/INL**



Measurement Results

- Power breakdown



total power
= 18.9mW

Performance Summary

Technology	65 nm CMOS
Supply Voltage	1.0 V
Sampling Rate	1.0 GS/s
Resolution	10 bit
Input Range	2.0 $V_{pp,diff}$
SNDR @ Nyquist	51.4 dB (8.2 ENOB)
DNL/INL	0.9 LSB / 1.1 LSB
Power	18.9 mW
FoM	62.3 fJ/step
Area	0.78 mm^2

Comparison

- **Comparison (f_s>0.8GS/s, SNDR>45dB, FoM <180fJ/step)**

	This work	ISSCC 2013 Hong	VLSI 2013 Chiang	VLSI 2012 Stepanovic	VLSI 2012 Sahoo	ISSCC 2011 Mulder
Architecture	TI SAR	TI SAR	PIPE	TI SAR	PIPE	TI PIPE
Technology	65nm	45nm	65nm	65nm	65nm	40nm
Supply Voltage (V)	1.0	1.2	1.0	1.2	1.2	1.0/2.5
Sampling rate (GS/s)	1.0	0.9	0.8	2.8	1.0	0.8
Resolution (bit)	10	9	10	11	10	12
SNDR @ Nyquist (dB)	51.4	51.2	52.2	48.2	52.4	59.0
Power (mW)	18.9	10.8	19.0	44.6	32.9	105
FoM (fJ/step)	62.3	40.5	71.4	75.8	96.6	180.2

Conclusions

- **A full-speed flash ADC is shared among 8 SAR channels**
- **Timing skew is estimated against the flash**
  - **Allows background calibration**
  - **No separate timing reference channel is needed**
- **The 65nm prototype ADC achieves the performance comparable to the state-of-art**
  - **Best FOM among GHz, 10 bit range ADCs in similar technology**

Acknowledgement

- MIT Center for Integrated Circuit and Systems
- Samsung Fellowship
- TSMC University Shuttle Program

A 1.62GS/s Time-Interleaved SAR ADC with Digital Background Mismatch Calibration Achieving Interleaving Spurs Below 70dBFS

Nicolas Le Dortz[1,2], Jean-Pierre Blanc[1], Thierry Simon[1], Sarah Verhaeren[1], Emmanuel Rouat[1], Pascal Urard[1], Stéphane Le Tual[1], Dimitri Goguet[1], Caroline Lelandais-Perrault[2], Philippe Benabes[2]

[1]STMicroelectronics, Crolles, France,
[2]Supélec, Gif-sur-Yvette, France

life.augmented

Supélec

Digital mismatch calibration motivation

NEED: High speed ADCs for high data rate communication

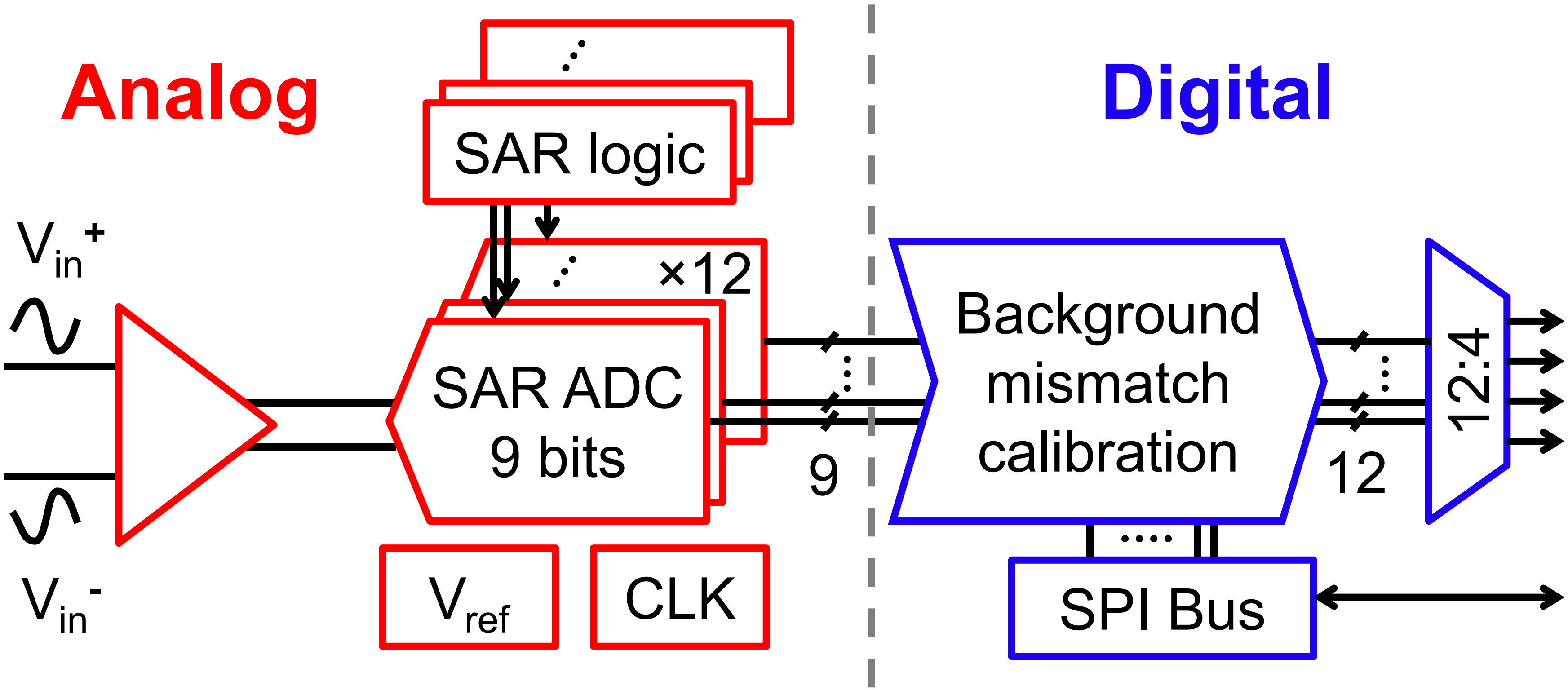
DESIGN CHOICE: Time-interleaved SAR ADCs

- High sampling frequency (multi-GS/s)
- Moderate resolution (up to 10 bits)
- Energy efficiency

ISSUES:

- **Mismatches** between the converters
- **Long development time** of mixed mismatch calibration architectures

Analog-digital co-design



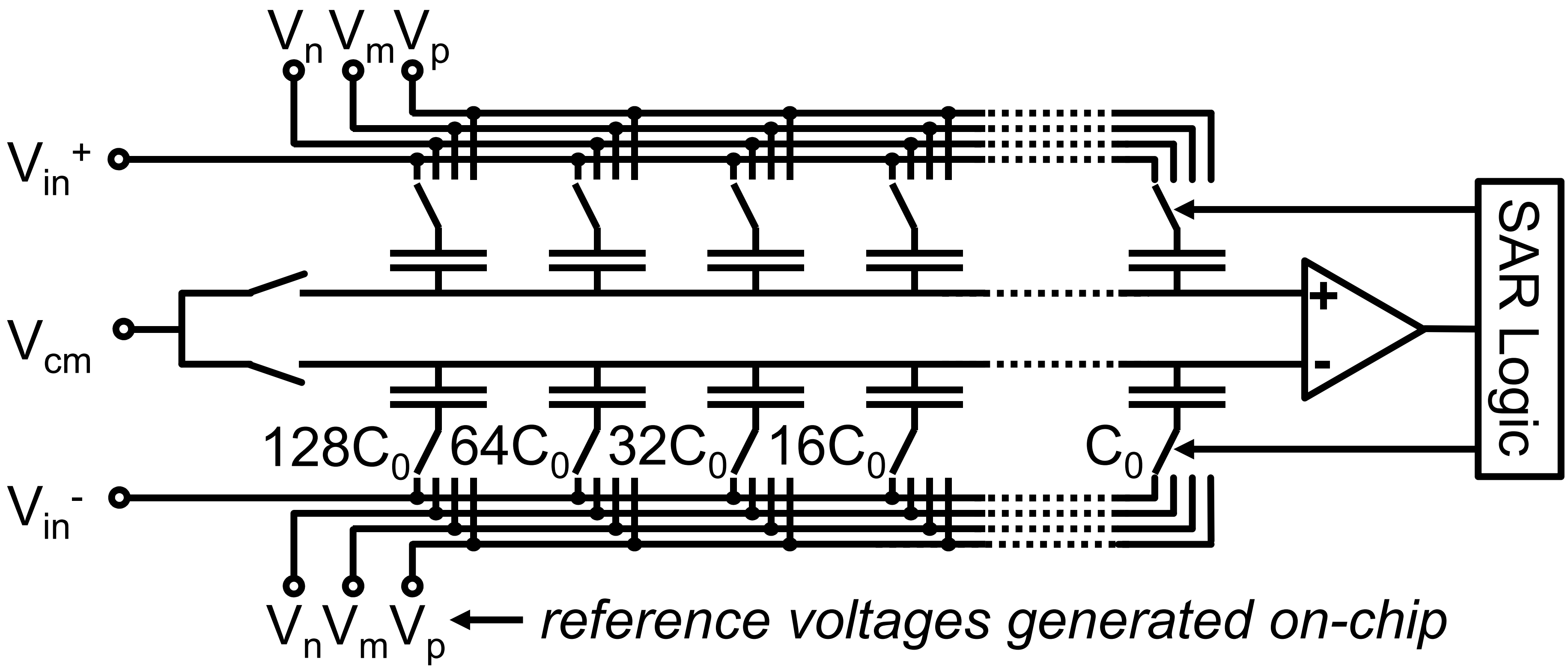
12 interleaved 9b-SAR ADCs @ F_S=1.62 GS/s

Digital mismatch calibration **w/o feedback** to analog

Outline

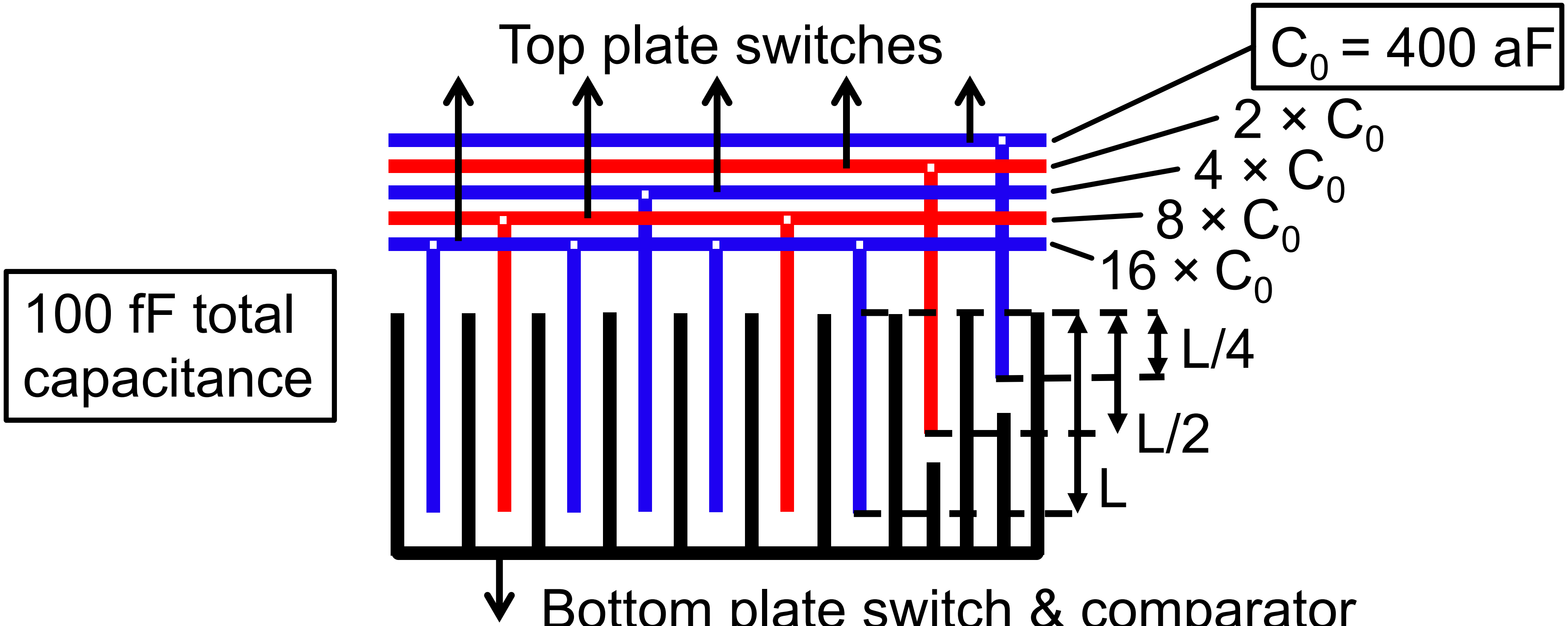
- **Analog architecture**
- Digital mismatch calibration
- Measurement results

Sub-ADC structure



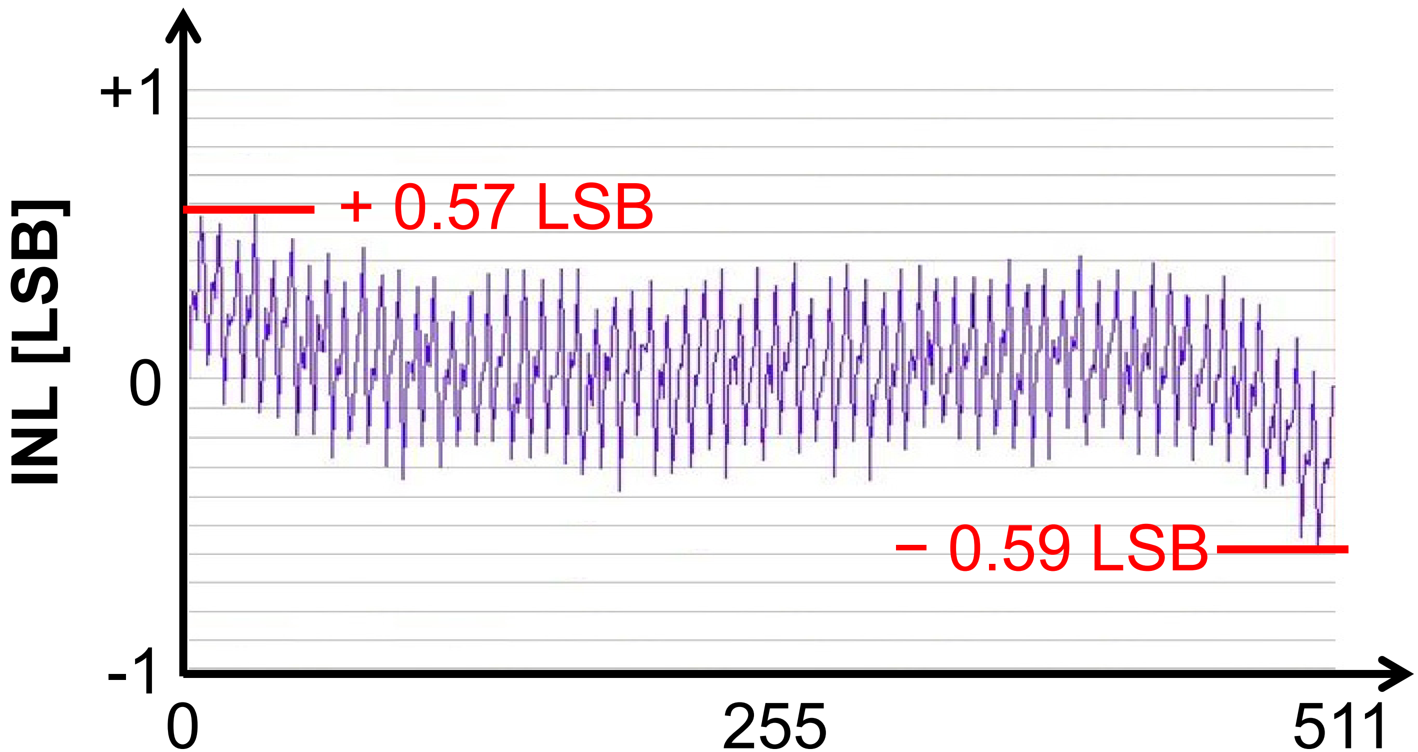
SAR ADC with radix-2 capacitive DAC
@ 135 MS/s for **high energy efficiency**

DAC capacitor array

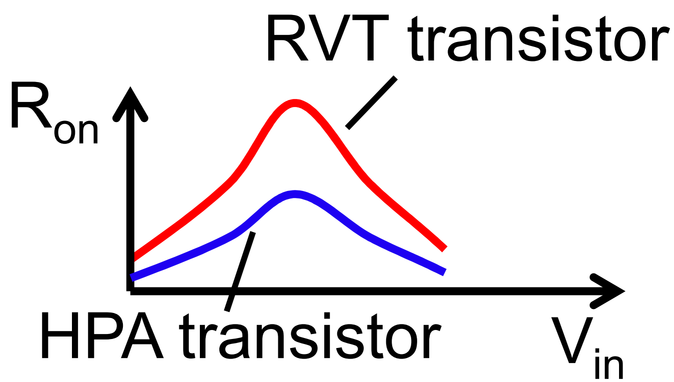


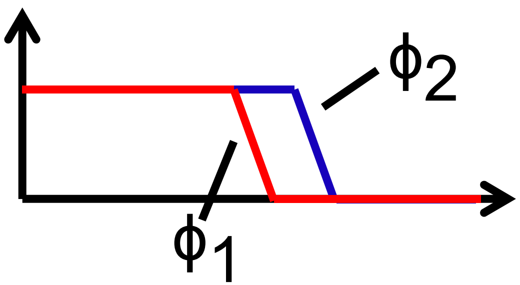
Custom 2-metal layout with **half & quarter fingers** reduces area

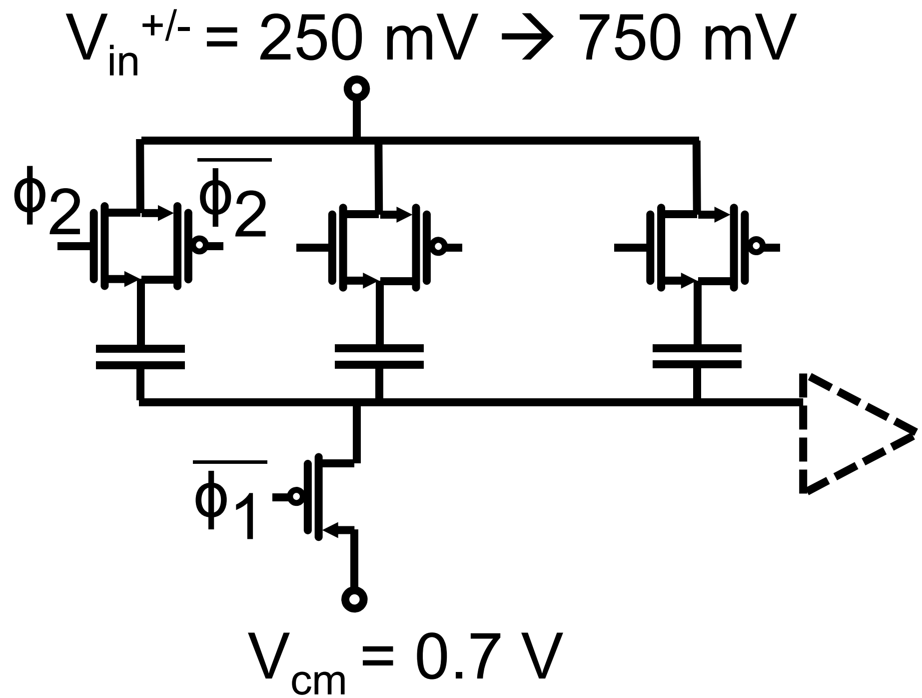
Capacitive DAC linearity



Sampling switch



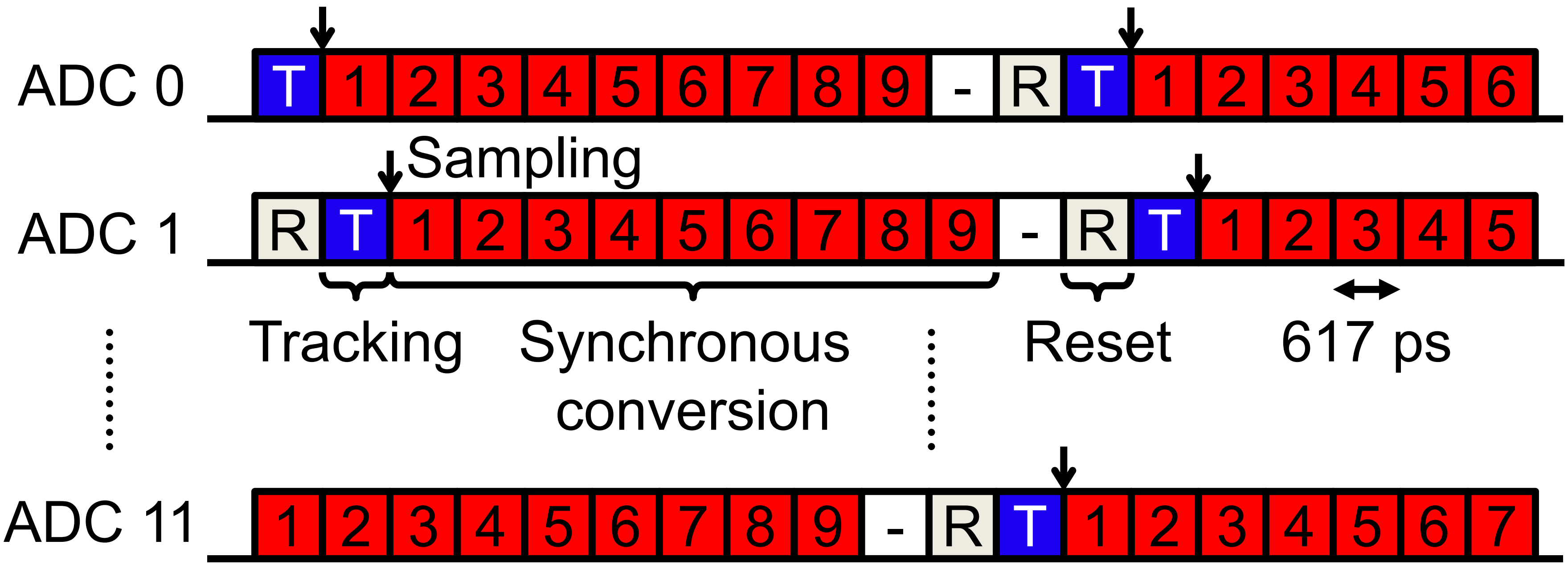




Linearity achieved through

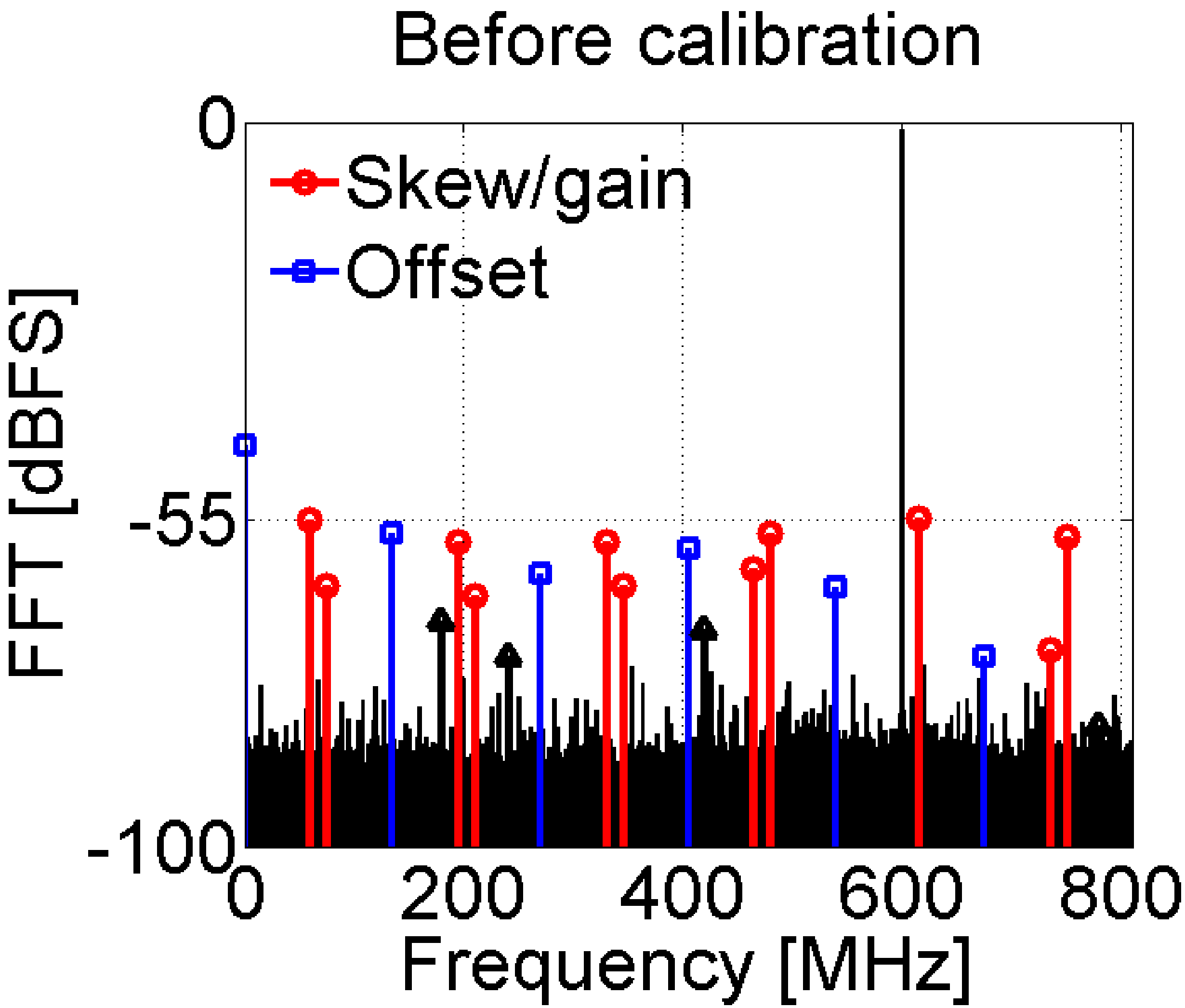
- Bottom plate sampling
- HPA low-V_t NMOS/PMOS transmission gate

Conversion operations



Custom SAR logic w/o standard cells enables **fast decisions**

Mismatch-limited ADC output

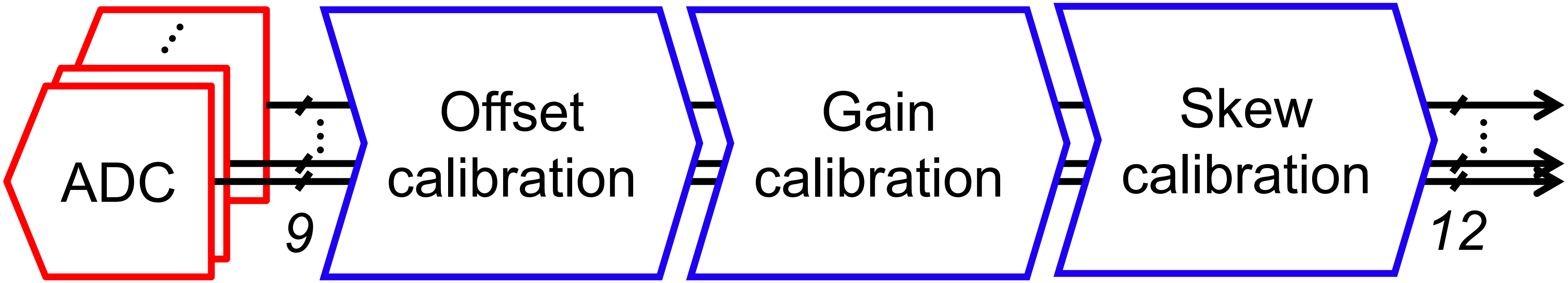


F_{in} = 600 MHz
F_s = 1.62 GHz

Outline

- Analog architecture
- **Digital mismatch calibration**
- Measurement results

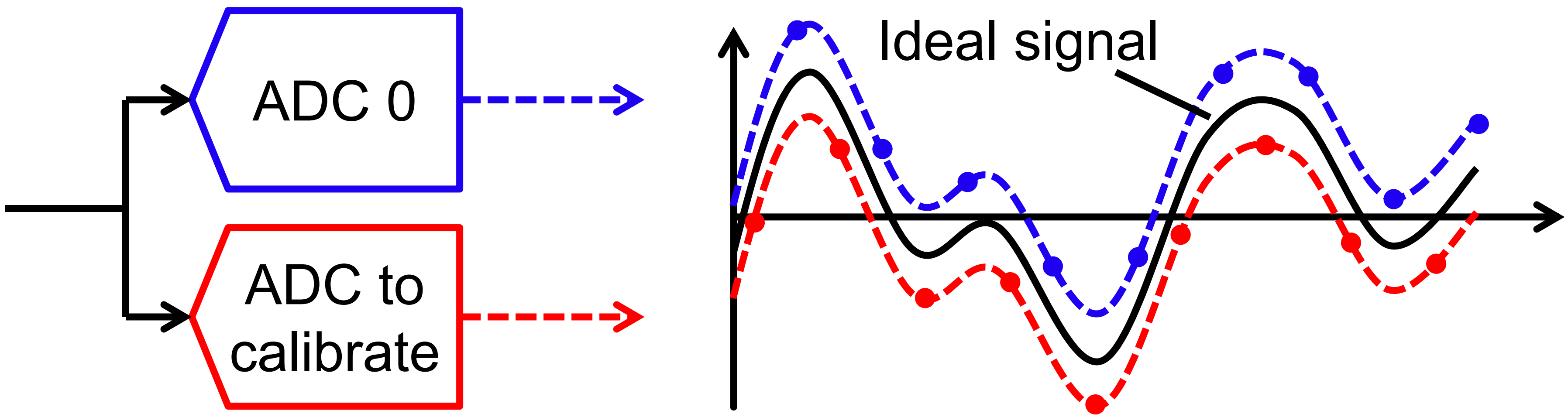
Digital mismatch calibration



- **Background** operation
  →Tracking of temperature and aging variations

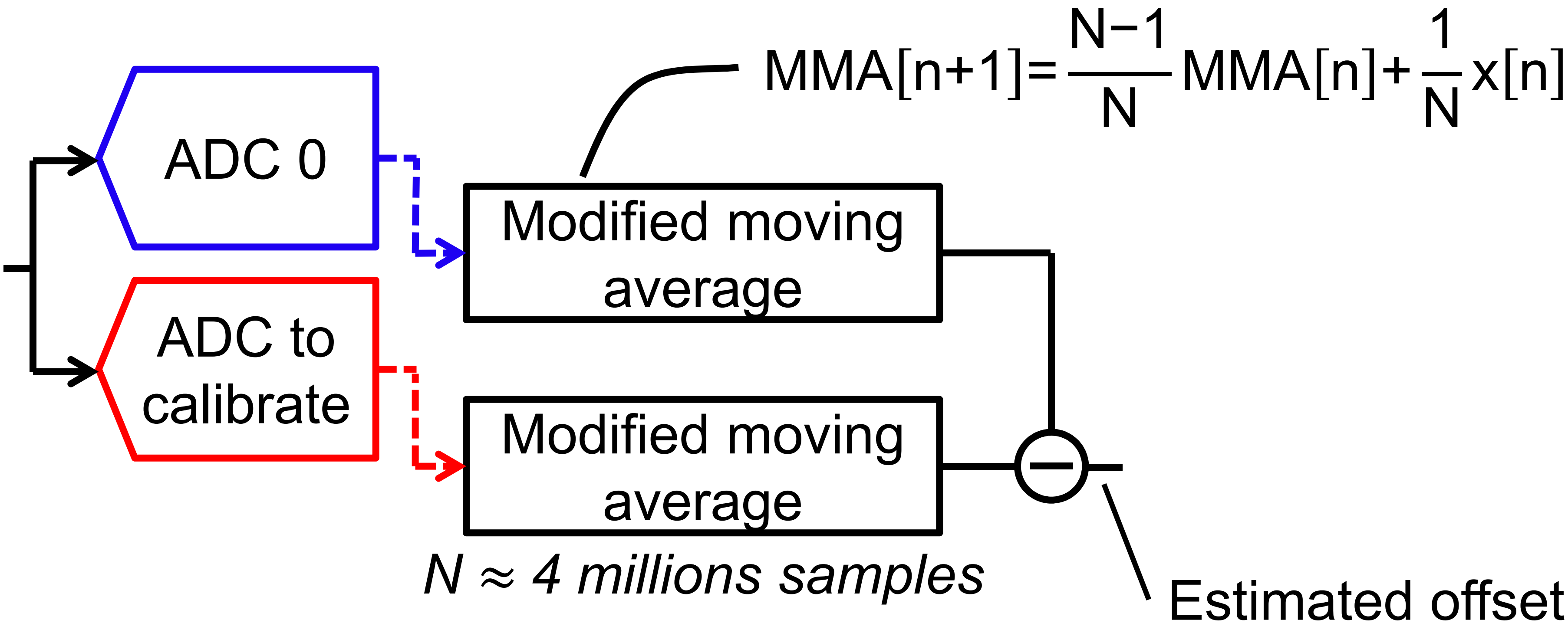
- Use of High Level Synthesis (HLS)
  - **Reusable**
  - **Parametric**
  - **Scalable**

Offset mismatch



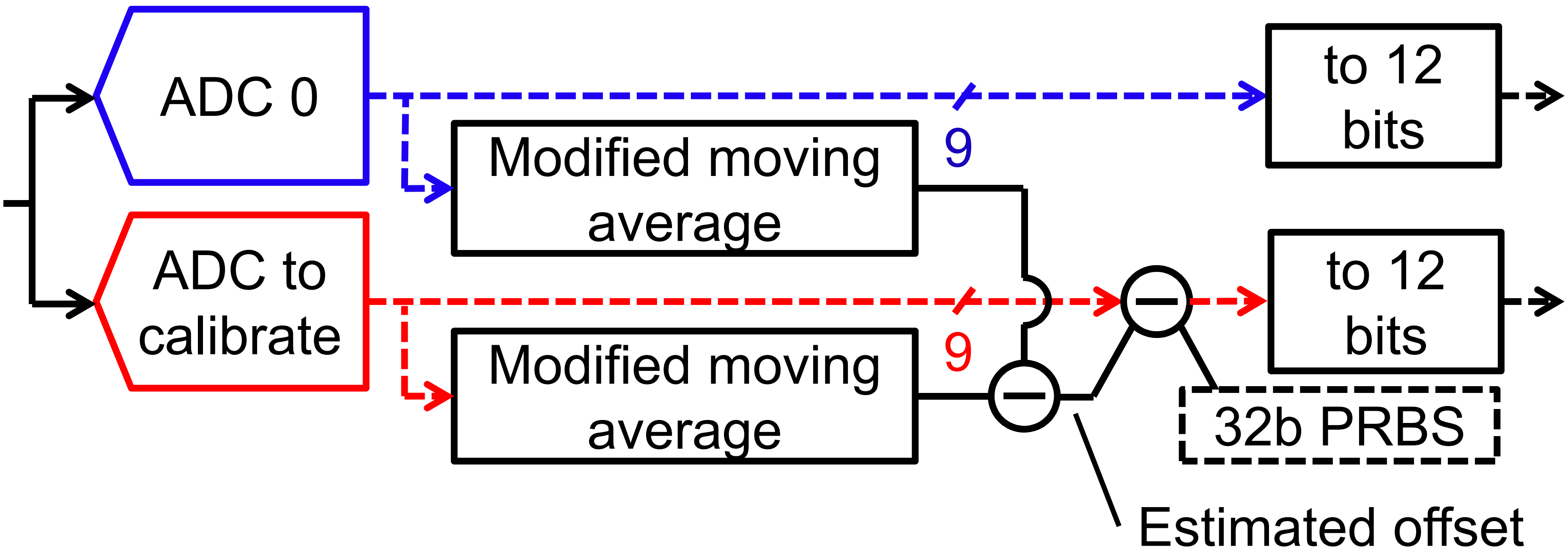
<u>Objective</u>: Digitally equalize the **offsets** of all ADCs

Offset mismatch estimation



<u>Requirement</u>: Wide Sense Stationary input signal

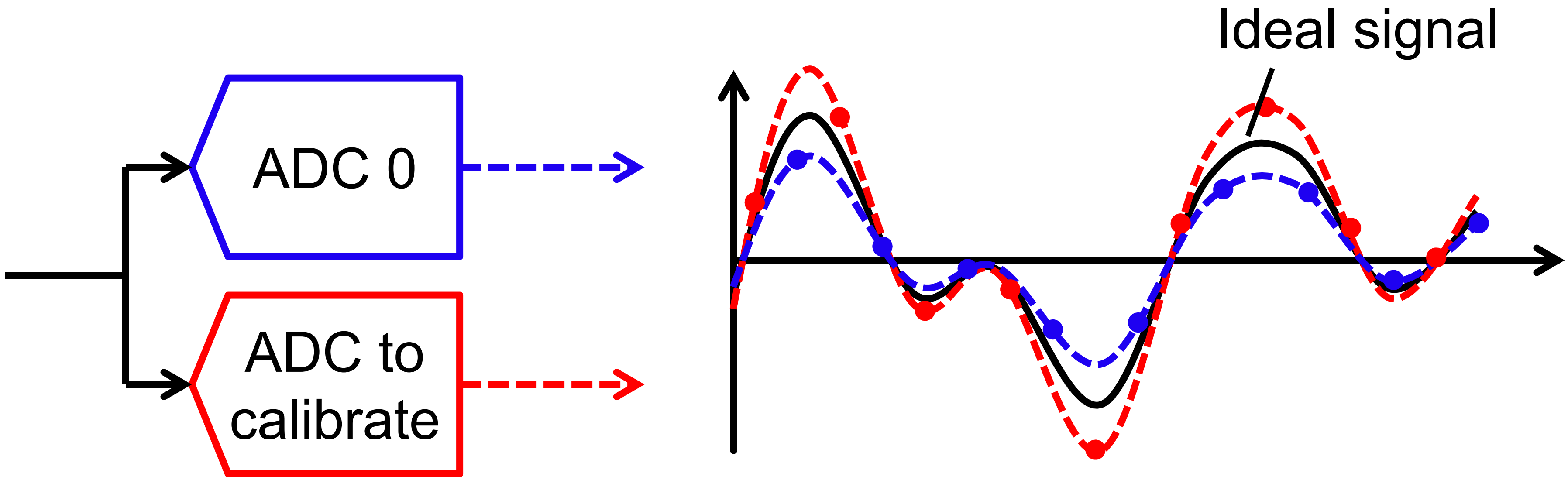
Full offset mismatch calibration



Reduction of rounding errors through

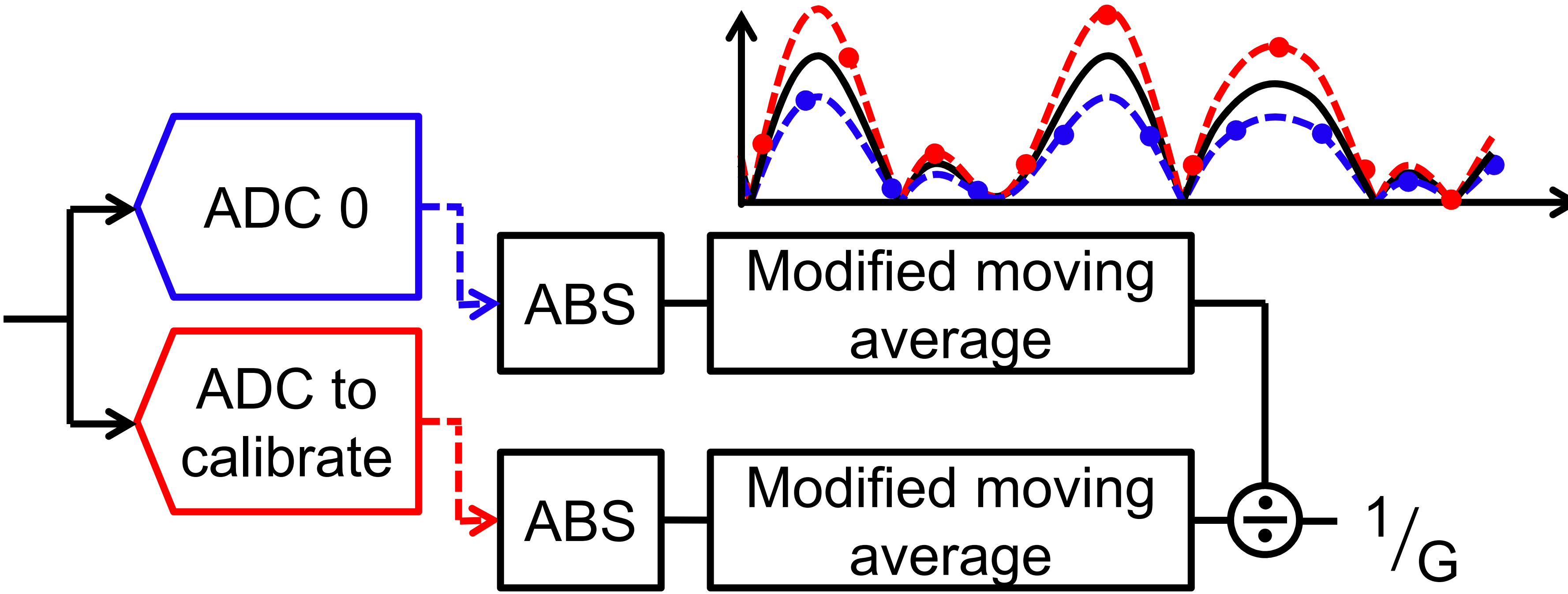
- 12b quantized output (3 bits added)
- Digital dithering to spread residual spurs

Gain mismatch



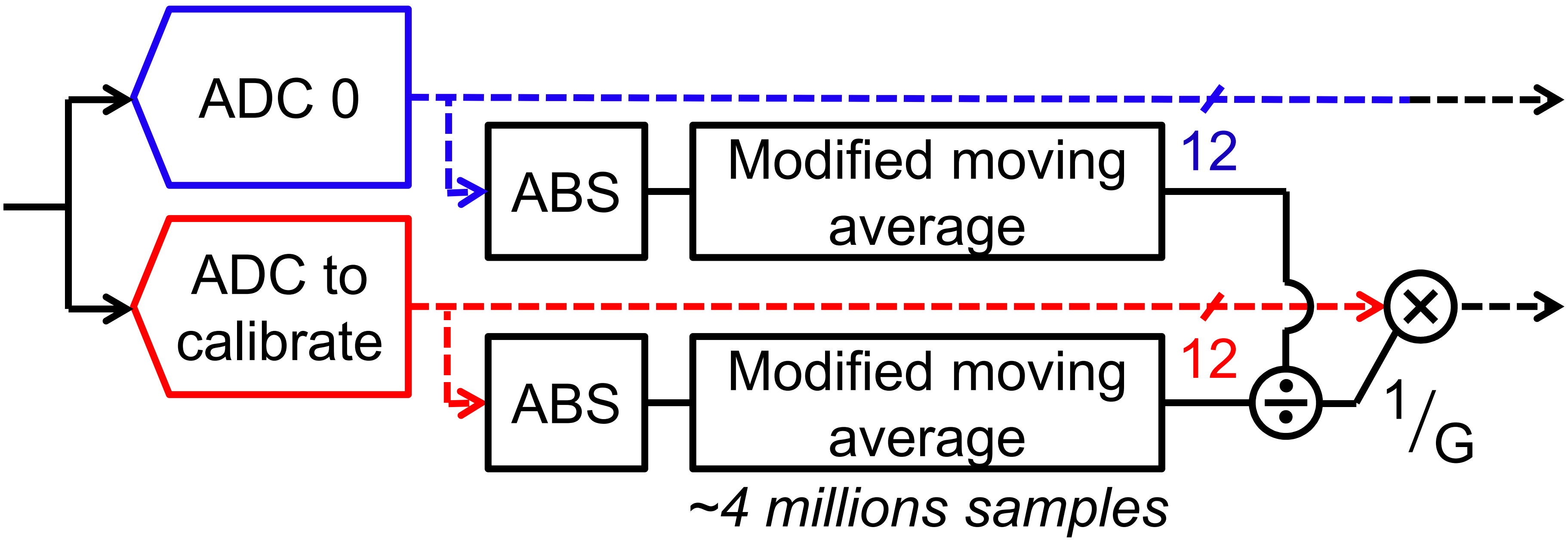
Objective: Digitally equalize the **gains** of all ADCs

Gain mismatch estimation

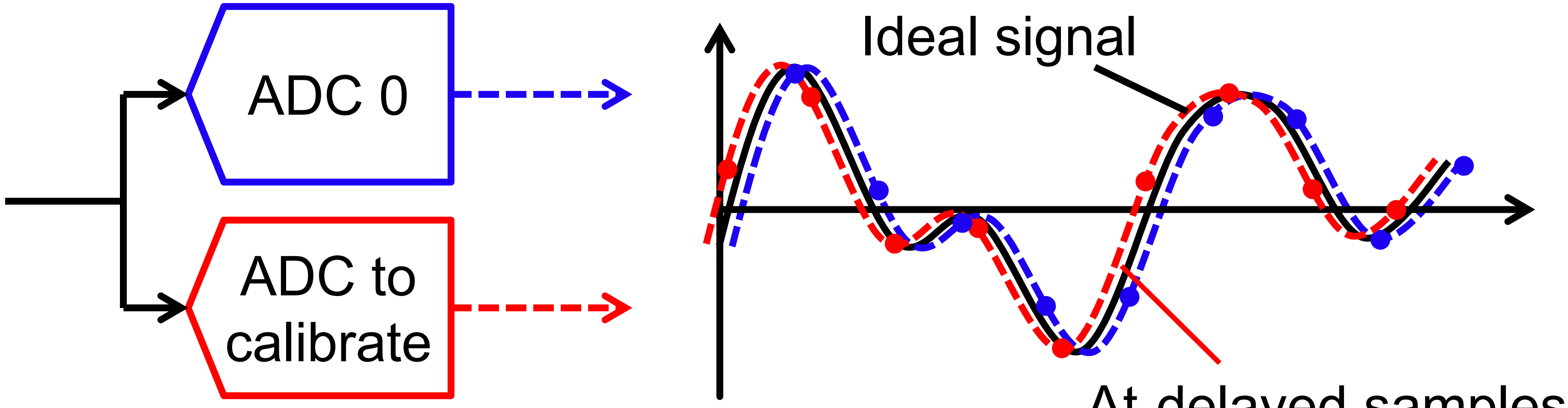


Absolute value → **low implementation cost** compared to squared value

Full gain mismatch calibration

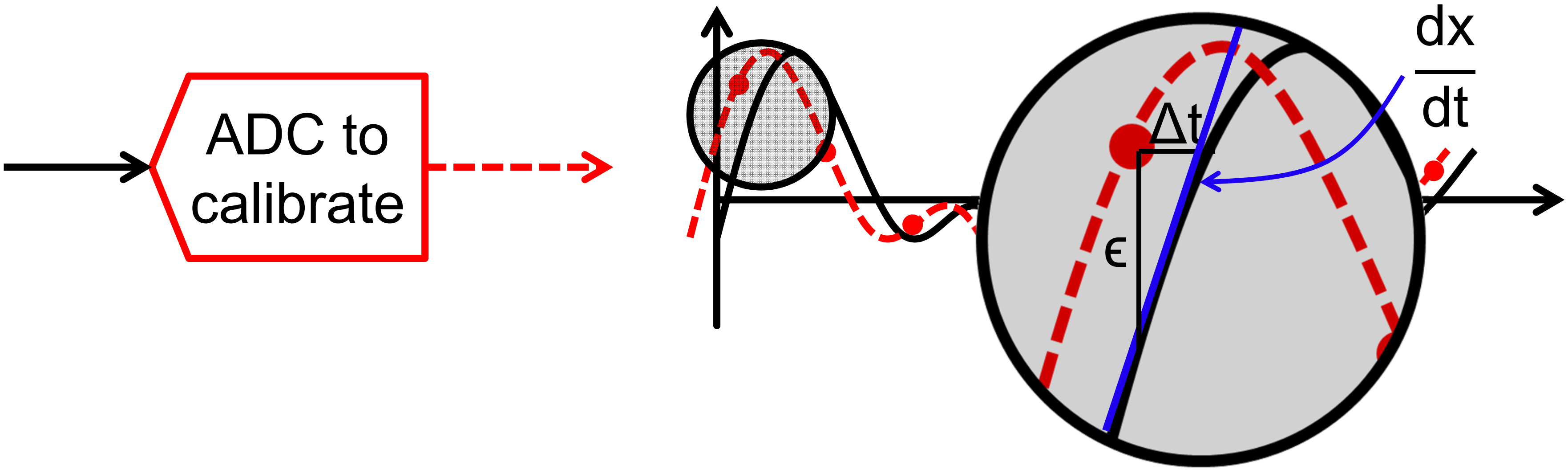


Skew mismatch



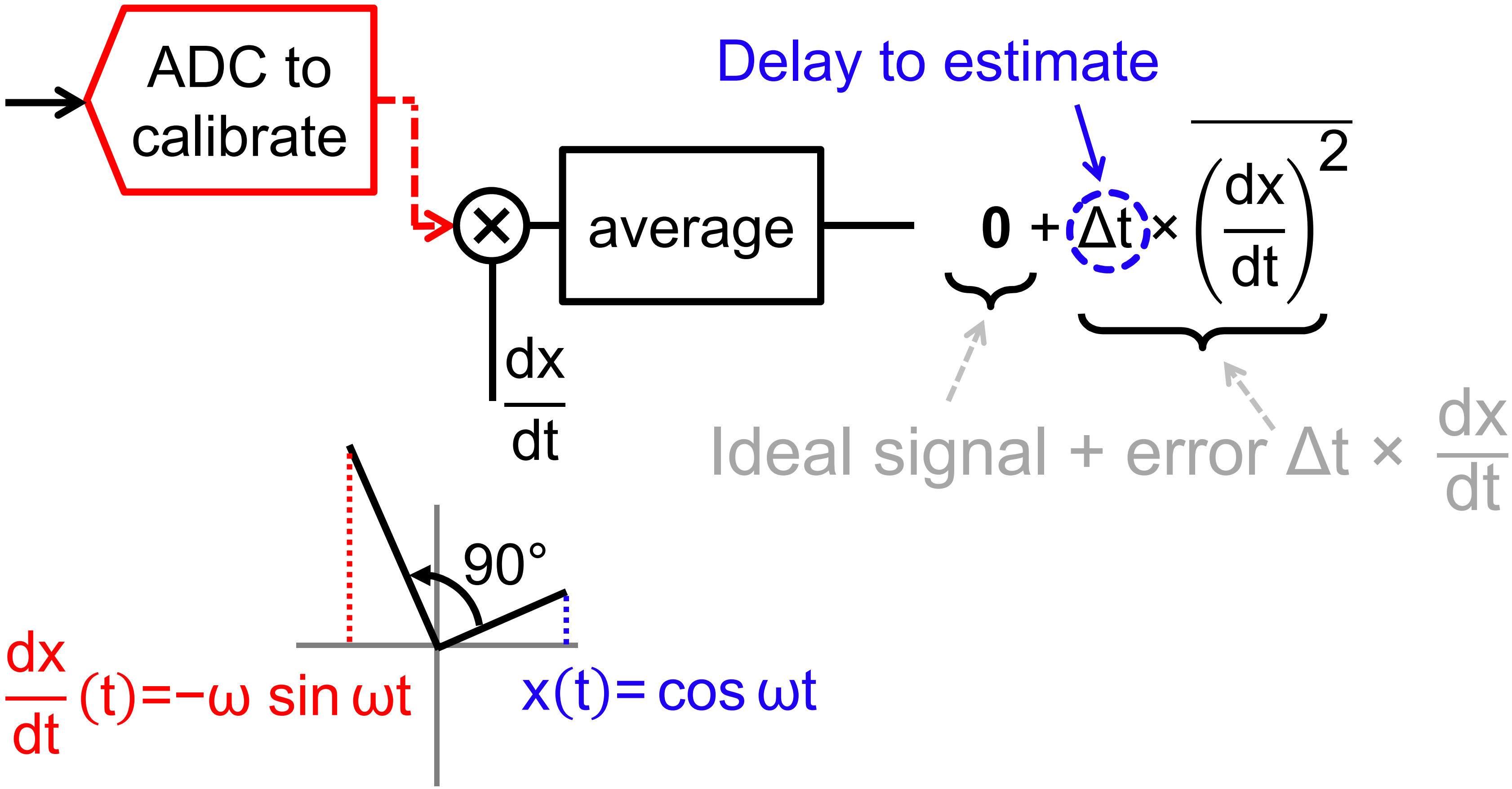
Objective: Digitally recover the correct **sampling times** of all ADCs

Skew mismatch error model



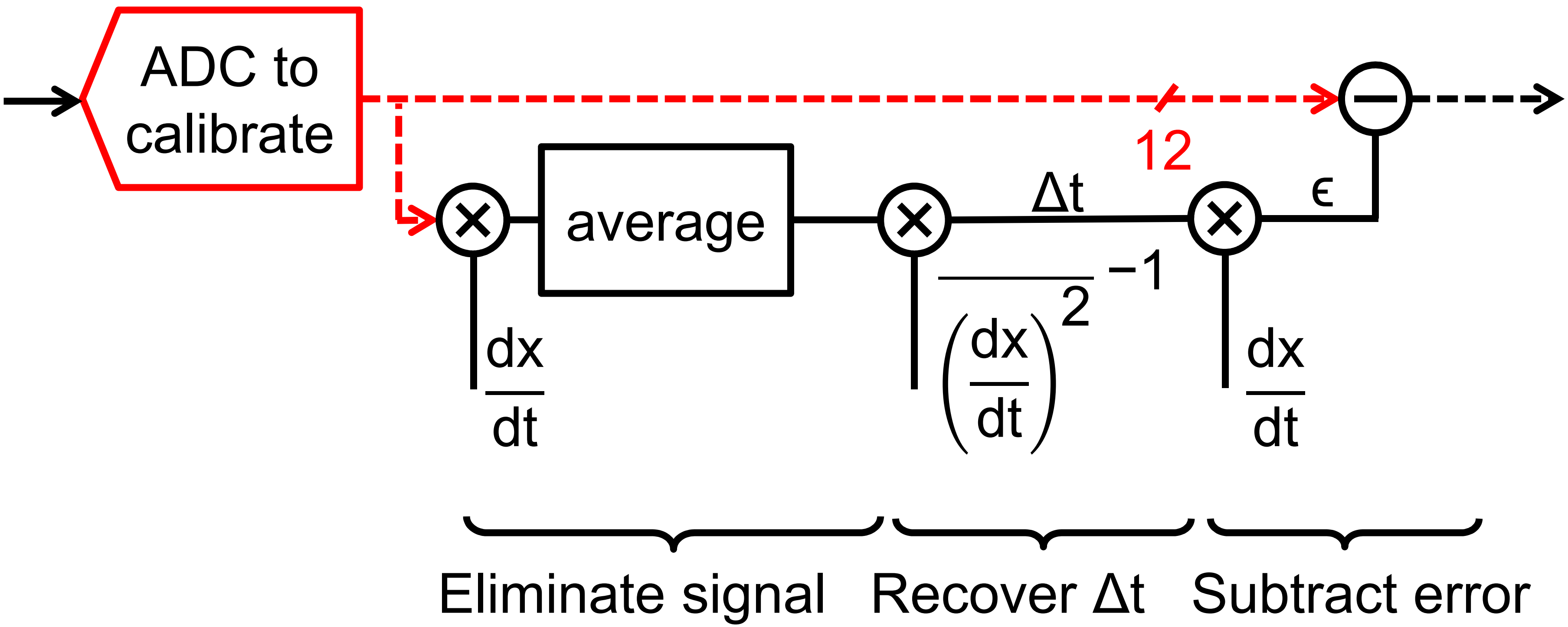
$$\text{Output ADC to calibrate} = \text{Ideal signal} + \underbrace{\textbf{error } \boldsymbol{\Delta t} \times \frac{\mathbf{dx}}{\mathbf{dt}}}_{\text{Term to eliminate}}$$

Signal-derivative orthogonality



Ideal signal term removed due to signal/derivative "orthogonality"

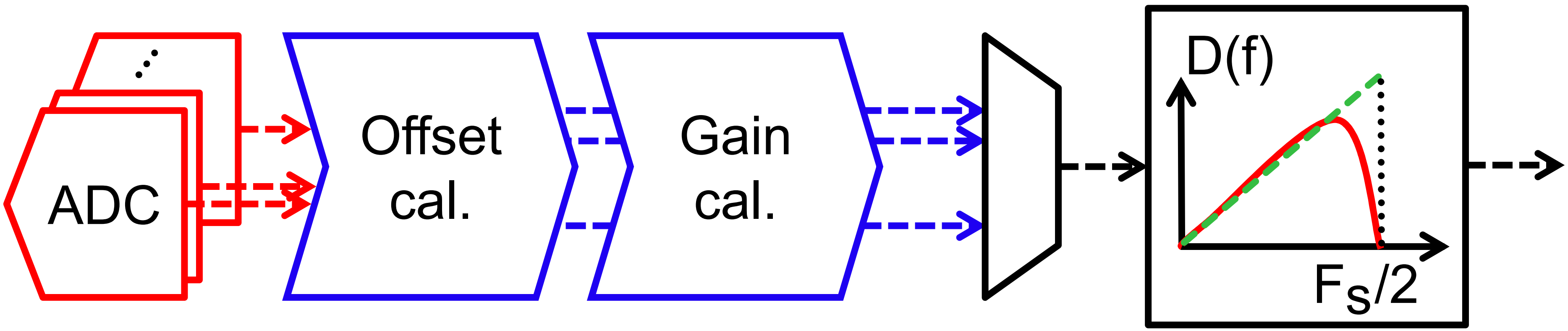
Full skew mismatch calibration



No feedback loop in the calibration

→No convergence issues

Digital derivative filter



Derivative filter

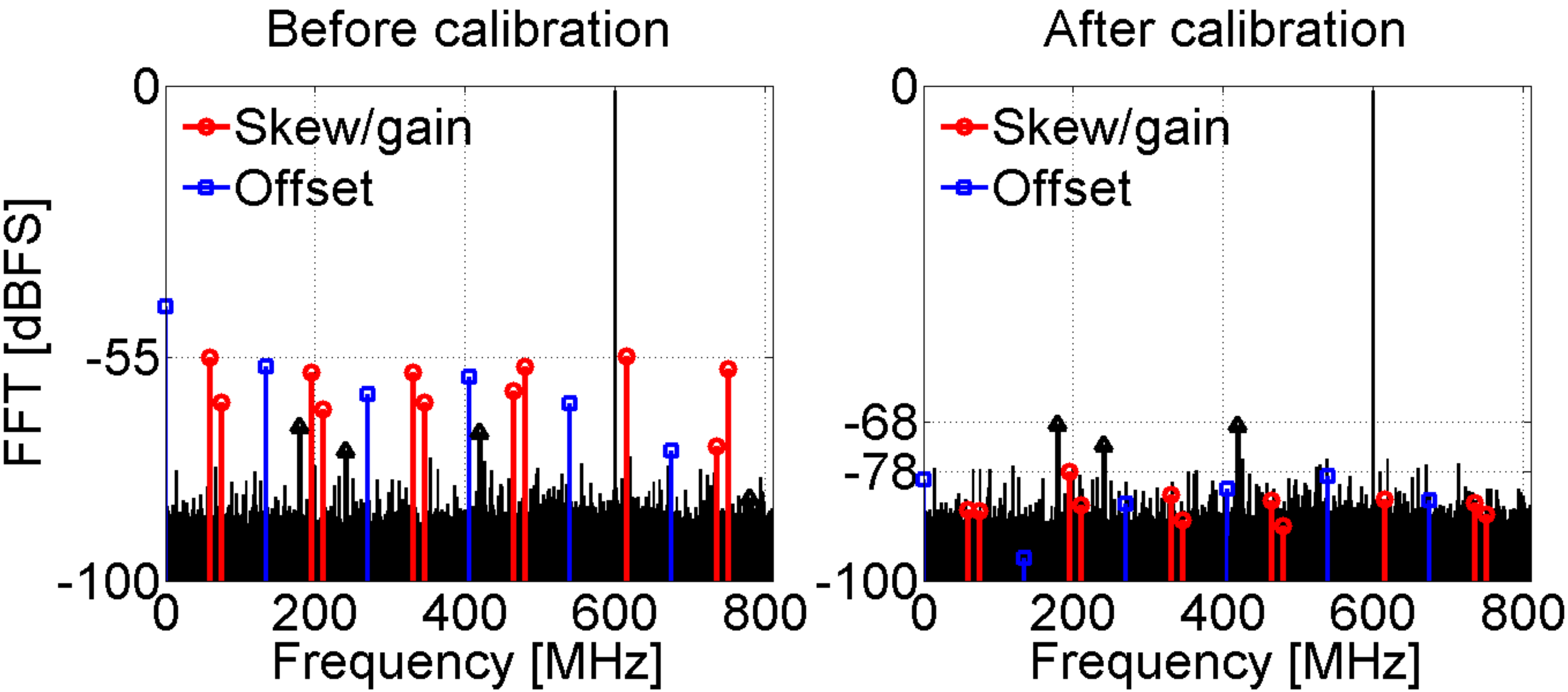
In this design: A 33-tap FIR filter with frequency response accurate up to 750 MHz

$$\boxed{d[n] = \frac{(-1)^n}{n},\ d[0] = 0} \quad + \text{ Hann window}$$

Outline

- Analog architecture
- Digital mismatch calibration
- **Measurement results**

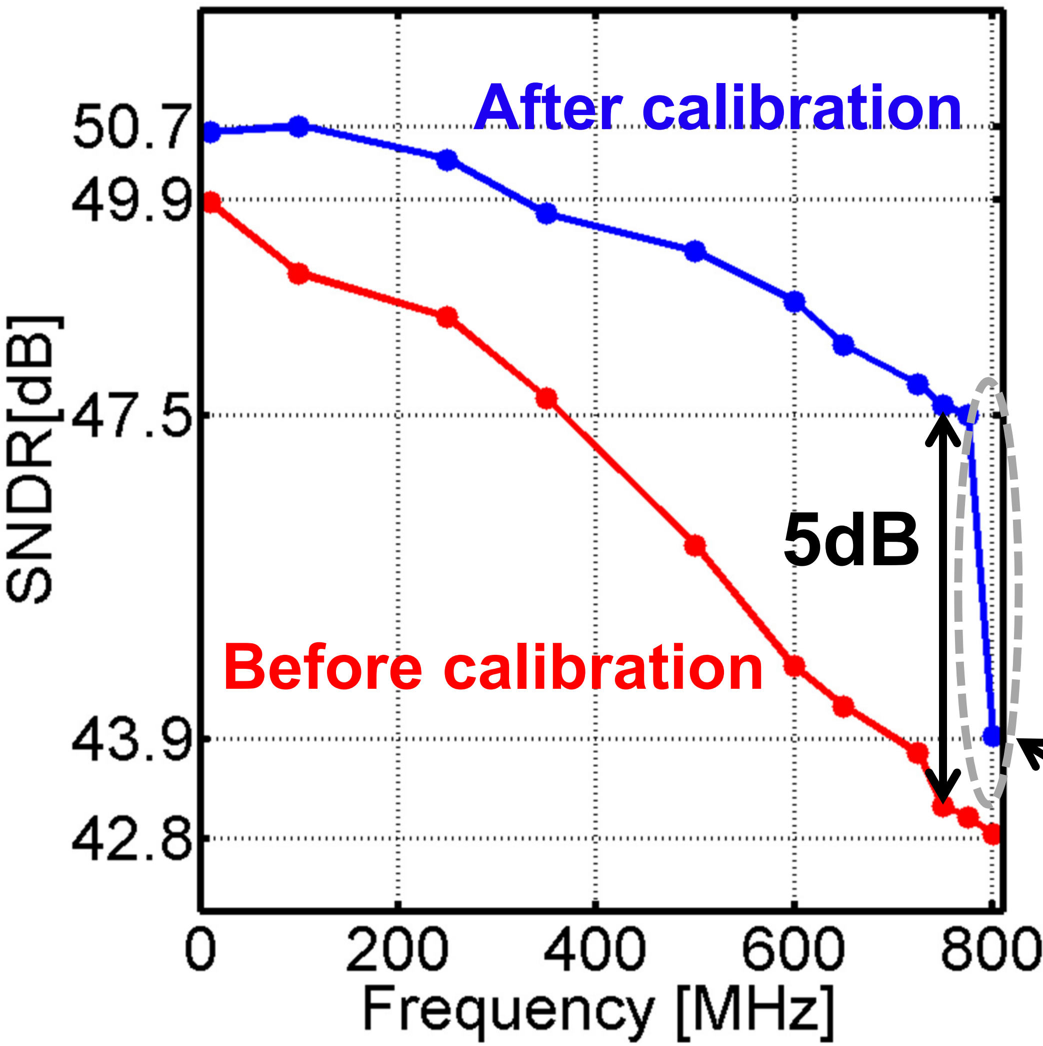
FFT Spectrum – Single tone



F_{in} = 600 MHz
F_s = 1.62 GHz

Offset spurs ↓23dB
Skew spurs ↓23dB

SNDR vs. input frequency



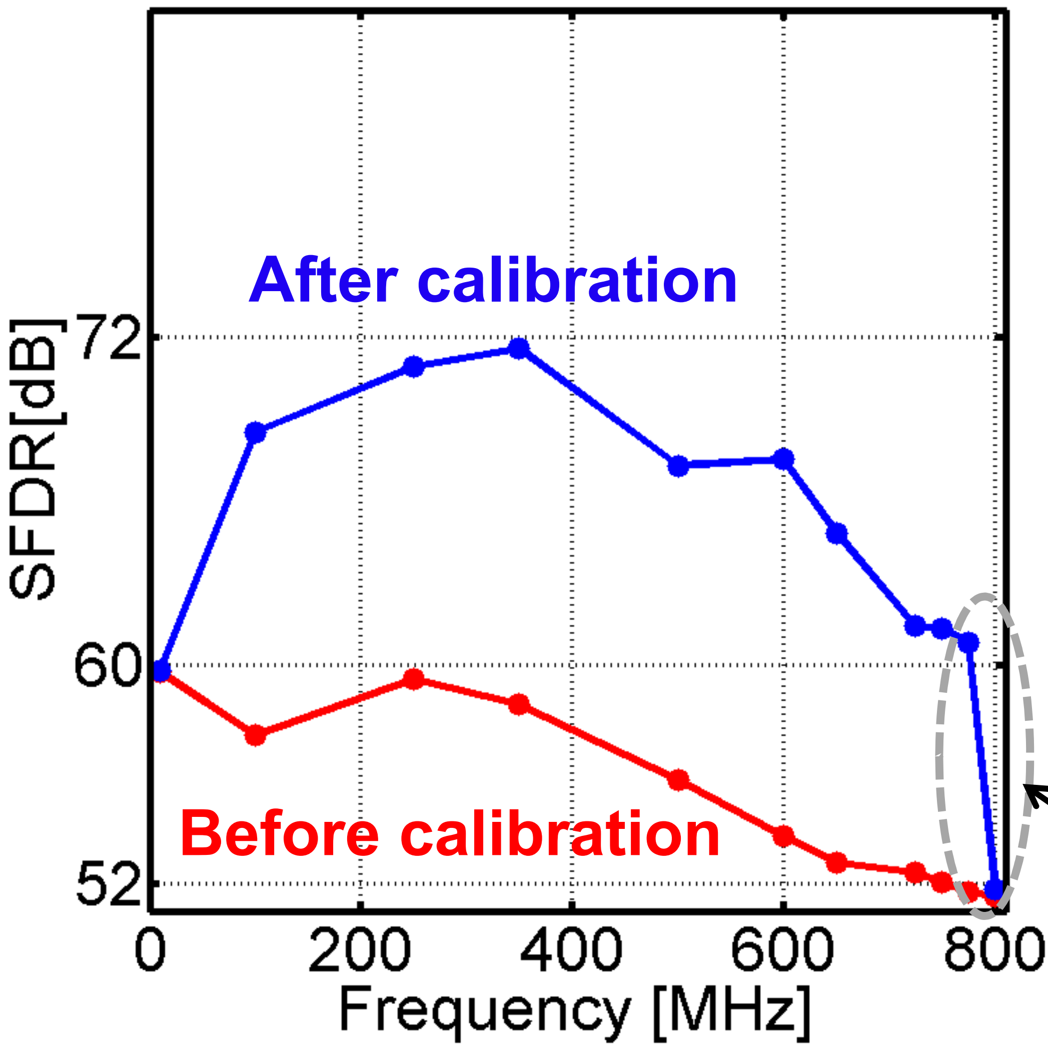
Sine input -1 dBFS

Key performance:

- Max. **SNDR 50.7 dB**
- **5dB = 0.83 ENOB** improvement at high input frequency

Derivative filter limitation

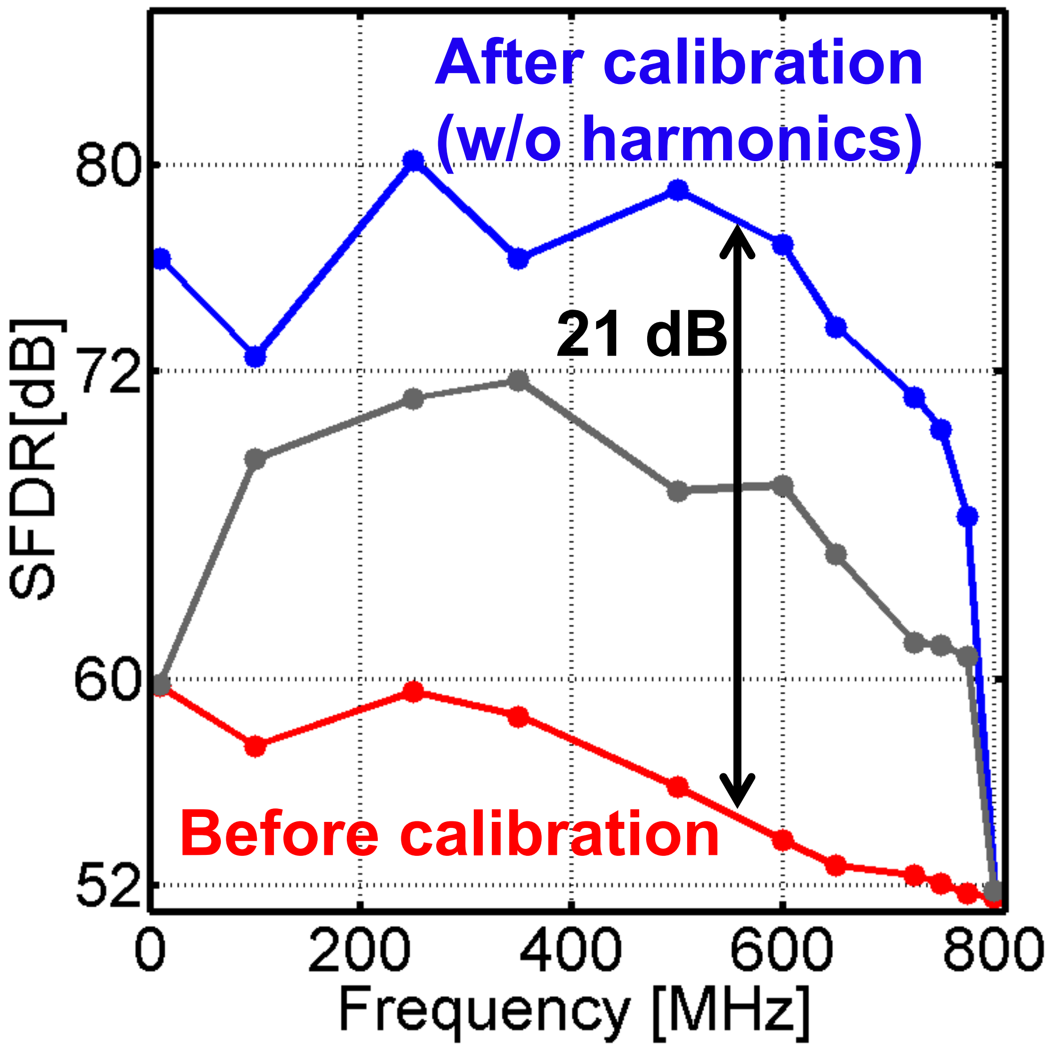
SFDR vs. input frequency



Up to 95% of Nyquist:
– **SFDR > 60 dB**

Derivative filter limitation

SFDR vs. input frequency

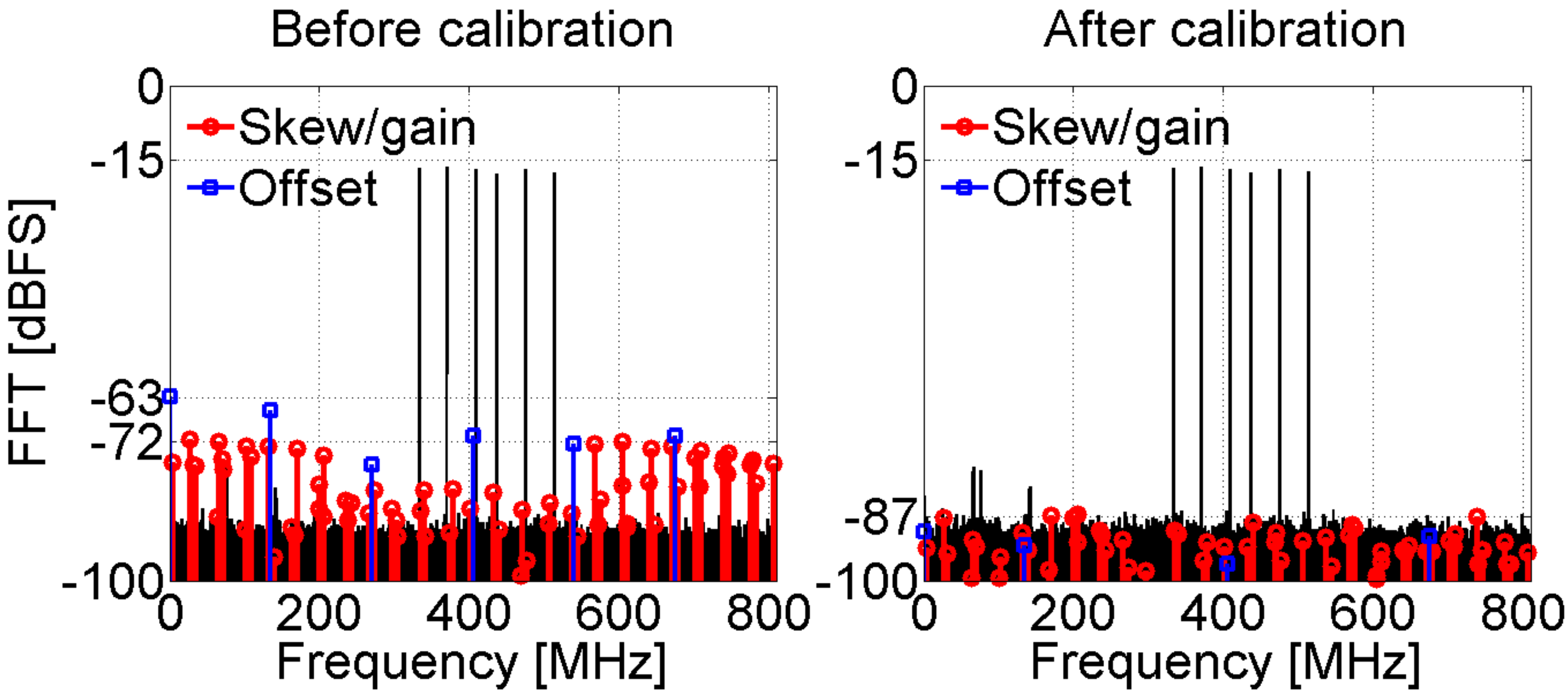


Linearity-limited SFDR

<u>Up to 95% of Nyquist:</u>

- SFDR > 60 dB
- **Mismatch spurs < 70 dBFS**

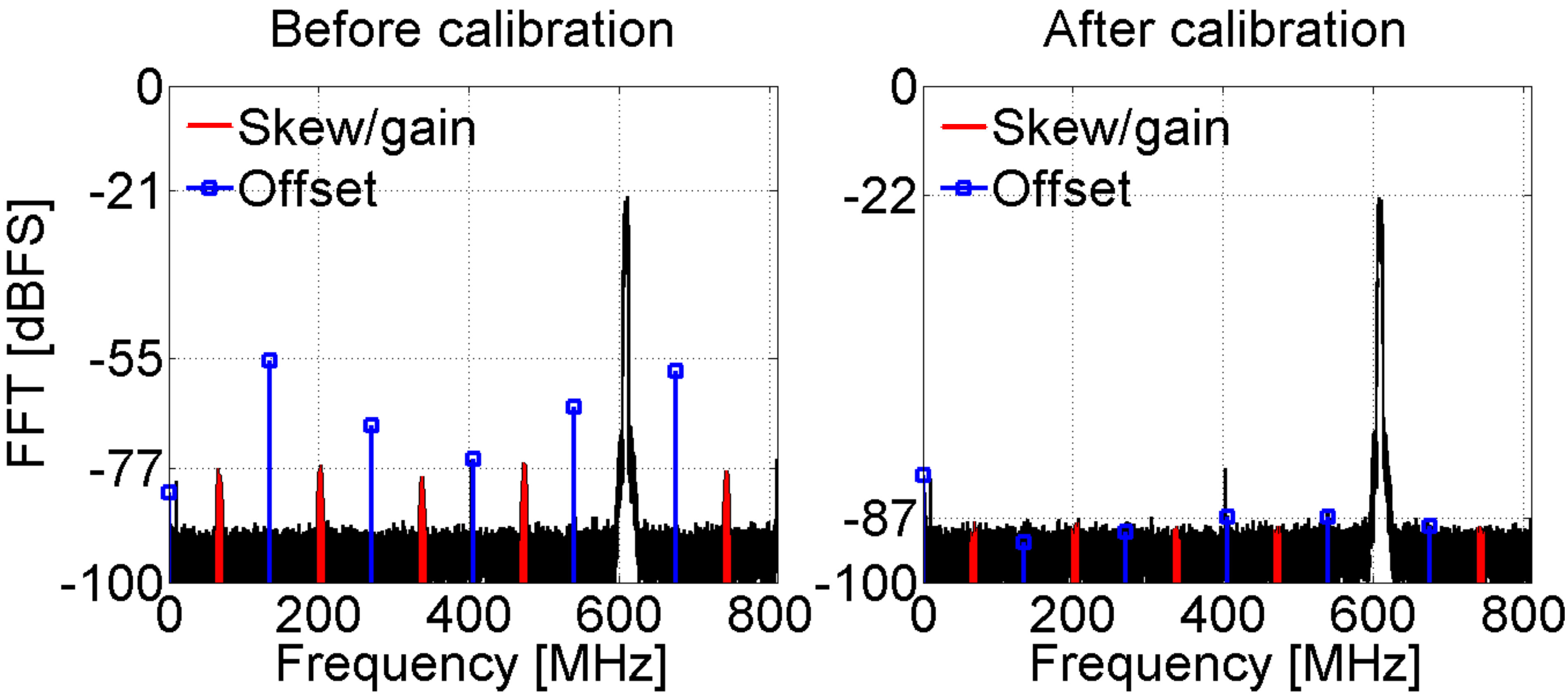
FFT Spectrum – Multitone signal



F_{in} = 334 → 513 MHz
F_s = 1.62 GHz

Offset spurs ↓25dB
Skew spurs ↓15dB

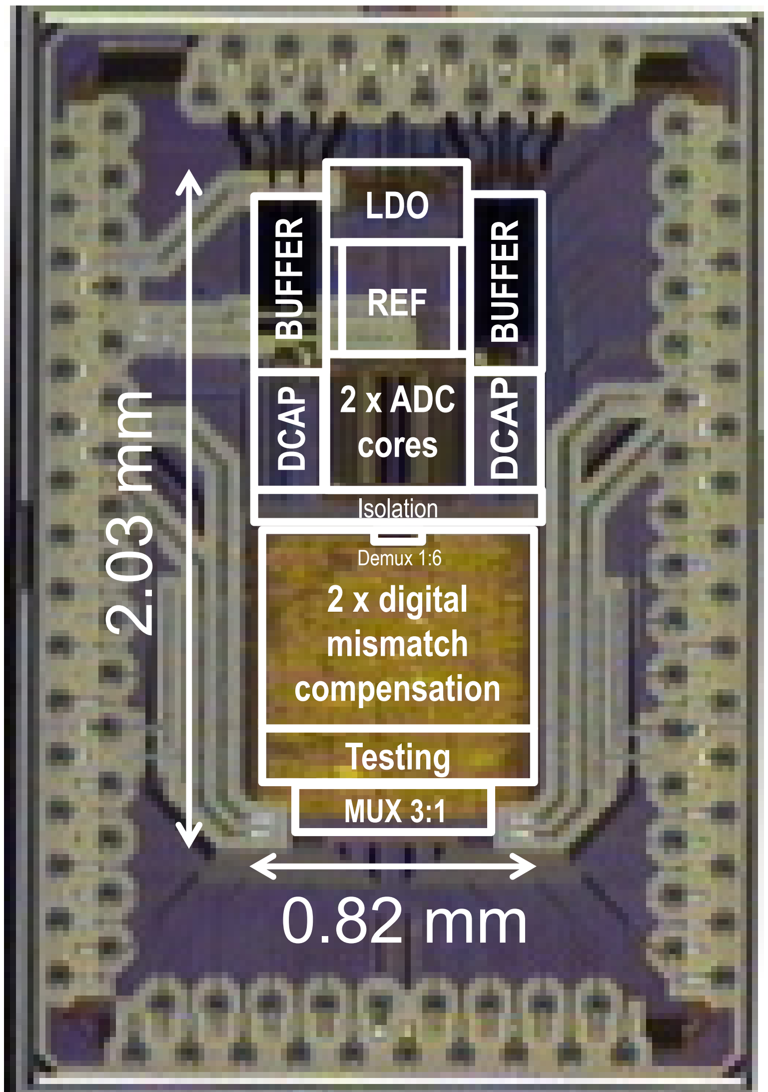
FFT Spectrum – Modulated signal



QAM16 modulation
$F_{carrier}$ = 607 MHz

Offset spurs ↓32dB
Gain/skew in noise floor

Chip fabrication

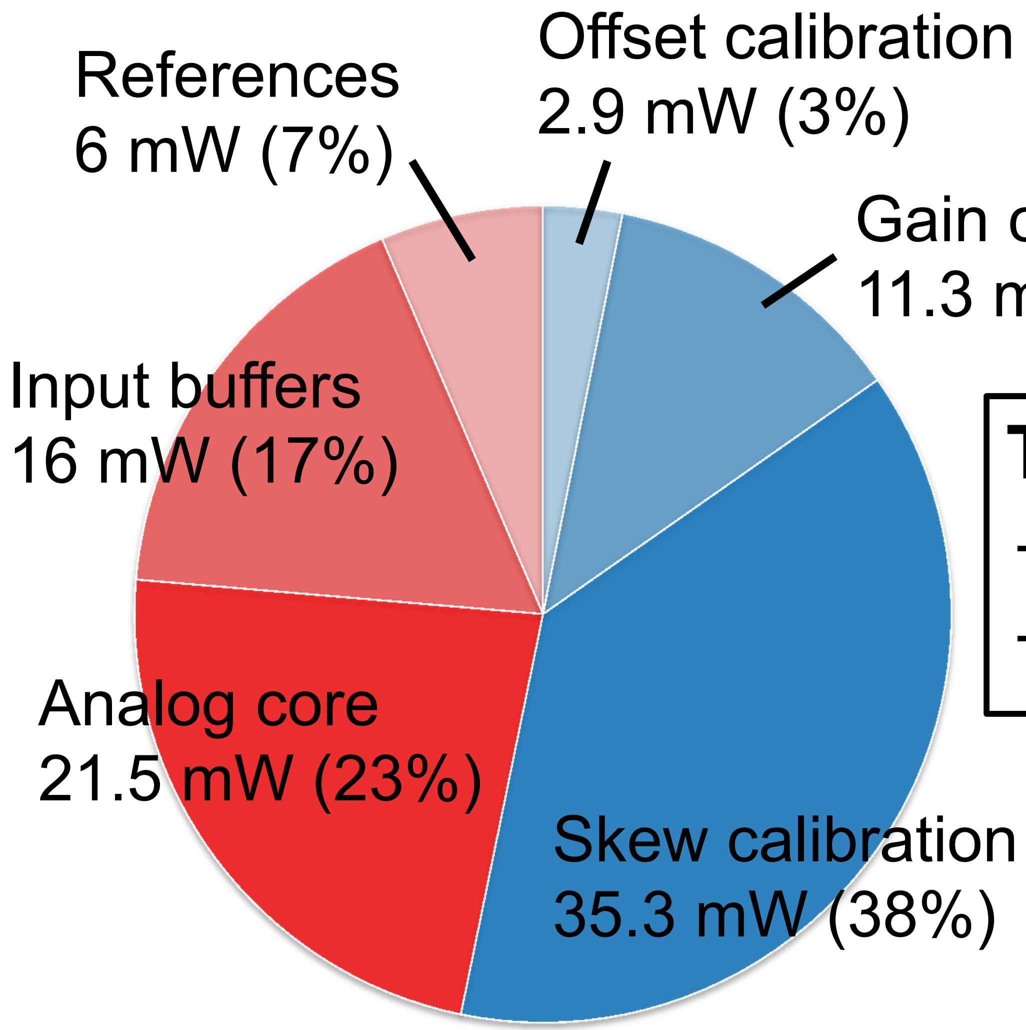


Technology: ST CMOS 40nm

1.66 mm^2 for 2 x TIADC

– Digital: 0.70 mm^2 (42%)
– Analog: 0.96 mm^2 (58%)

Power consumption



Total per TIADC: 93mW

- Analog: 43.5 mW
- Digital: 49.5 mW

Performance vs. previous work

	[1]	[2]	[3]	This work
Technology	65nm	65nm	65nm	40nm
Sampling rate [GS/s]	3.6	2.6	2.8	1.6
Mismatch tones [dBFS]	50	55	60	**70**
SFDR [dBFS]	50	55	55	62
THD [dB]	-55	-58	-55	-58
SNDR [dB]	47	49	48	48
Power [mW]	795	480	44.6	93
FOM [fJ/conv]	1207	801	76	283
Area [mm²]	7.4	5.1	0.63	0.83

[1] Janssen, ISSCC 2013
[2] Doris, ISSCC 2011
[3] Stepanovic, VLSI 2011

Conclusion

- Successful analog/digital co-design with **low development time**
- Background digital mismatch calibration
  - **Reusable**
  - **Parametric**
  - **Scalable**

Acknowledgements

- Co-authors from ST and Supélec
- Andreia Cathelin (ST)
- Borivoje Nikolić (BWRC)
- Filipe Vinci (Supélec)
- BWRC students

A 2.2GS/s 7b 27.4mW Time-Based Folding-Flash ADC with Resistively Averaged Voltage-to-Time Amplifiers

Masaya Miyahara, Ibuki Mano, Masaaki Nakayama, Kenichi Okada, and Akira Matsuzawa

Tokyo Institute of Technology, Japan

Matsuzawa & Okada Lab.

TOKYO TECH
Pursuing Excellence

Outline

- Motivation
- Design concepts
  - Time-based folding architecture
  - Voltage-to-time amplifier
- Measurement results
- Conclusion

Motivation

Flash ADCs

☺ Highest conversion rate and lowest latency

⇒ High speed feedback-loop systems

☹ Power and area are proportional to the number of comparators

Folding-Flash ADCs

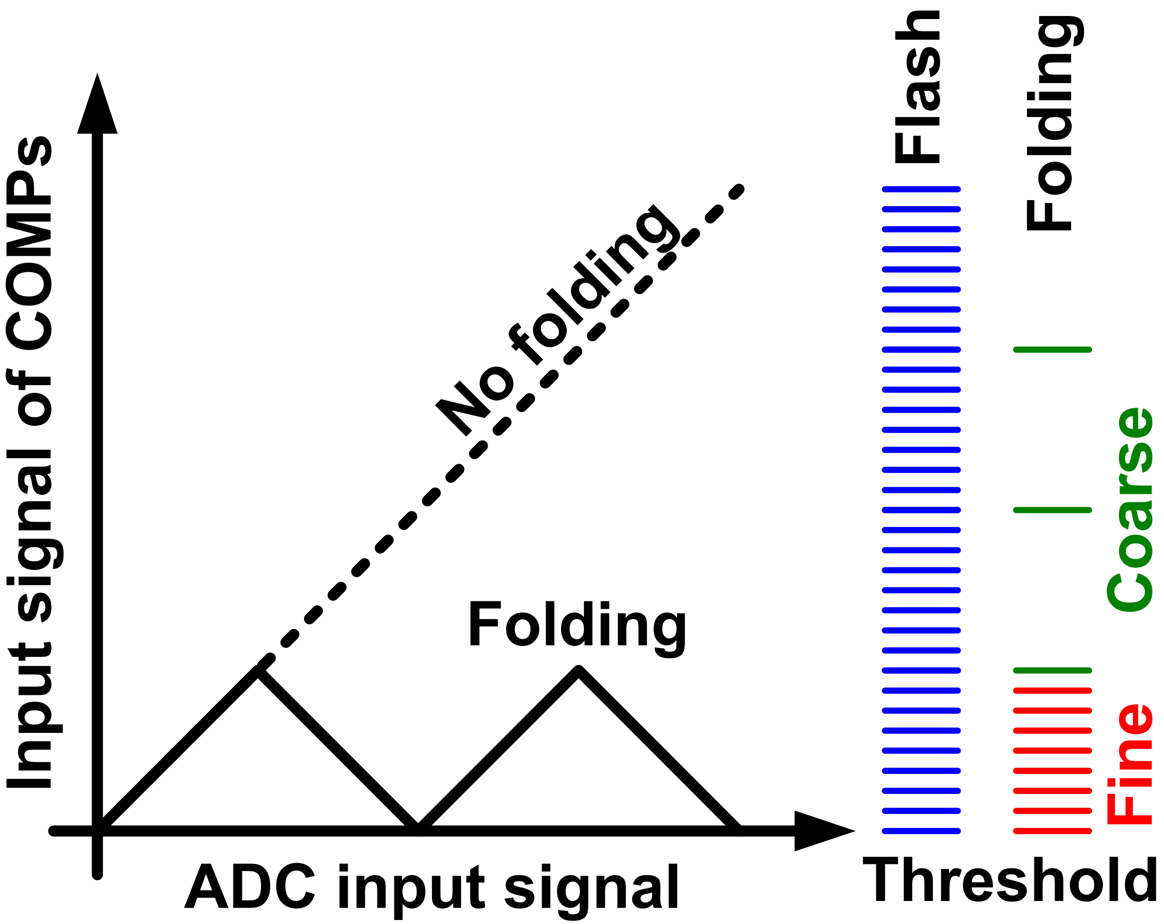
☺ Less number of comparators

☹ Power consuming of amplifiers in the folding circuit[1, 2]

New efficient folding architecture is required

[1] Y. Nakajima, *et al.*, JSSC 2010 [2] T. Yamase, *et al.*, VLSI symp. 2011

Conventional Folding-Flash ADC



N : Resolution [bit]

Folding times

2^{M}-1

Number of Comps

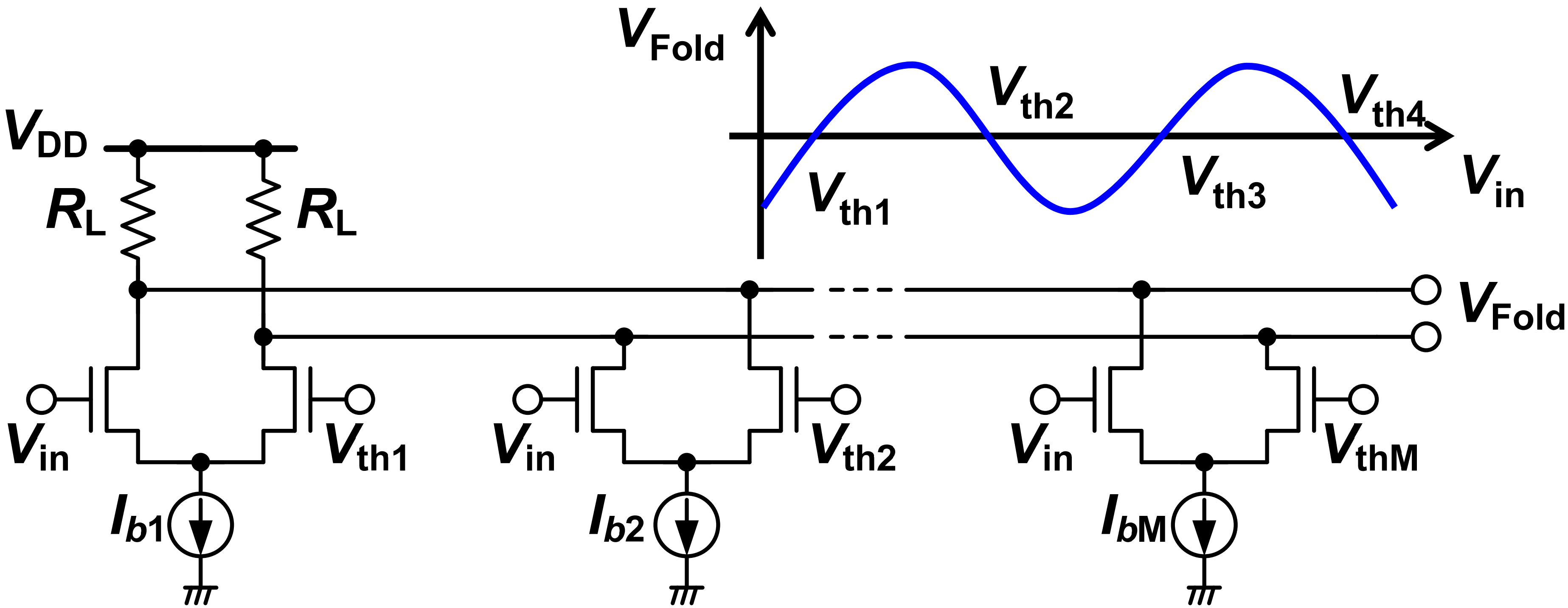
$\underbrace{2^{M}}_{\text{Coarse}} + \underbrace{2^{N-M+1}}_{\text{Fine}}$

N=7bit, M=4

128⇒32

Conventional Folding Circuit

- Large current is needed for high speed
- Voltage gain is reduced by technology scaling



New Design Concepts

Time-based-folding architecture

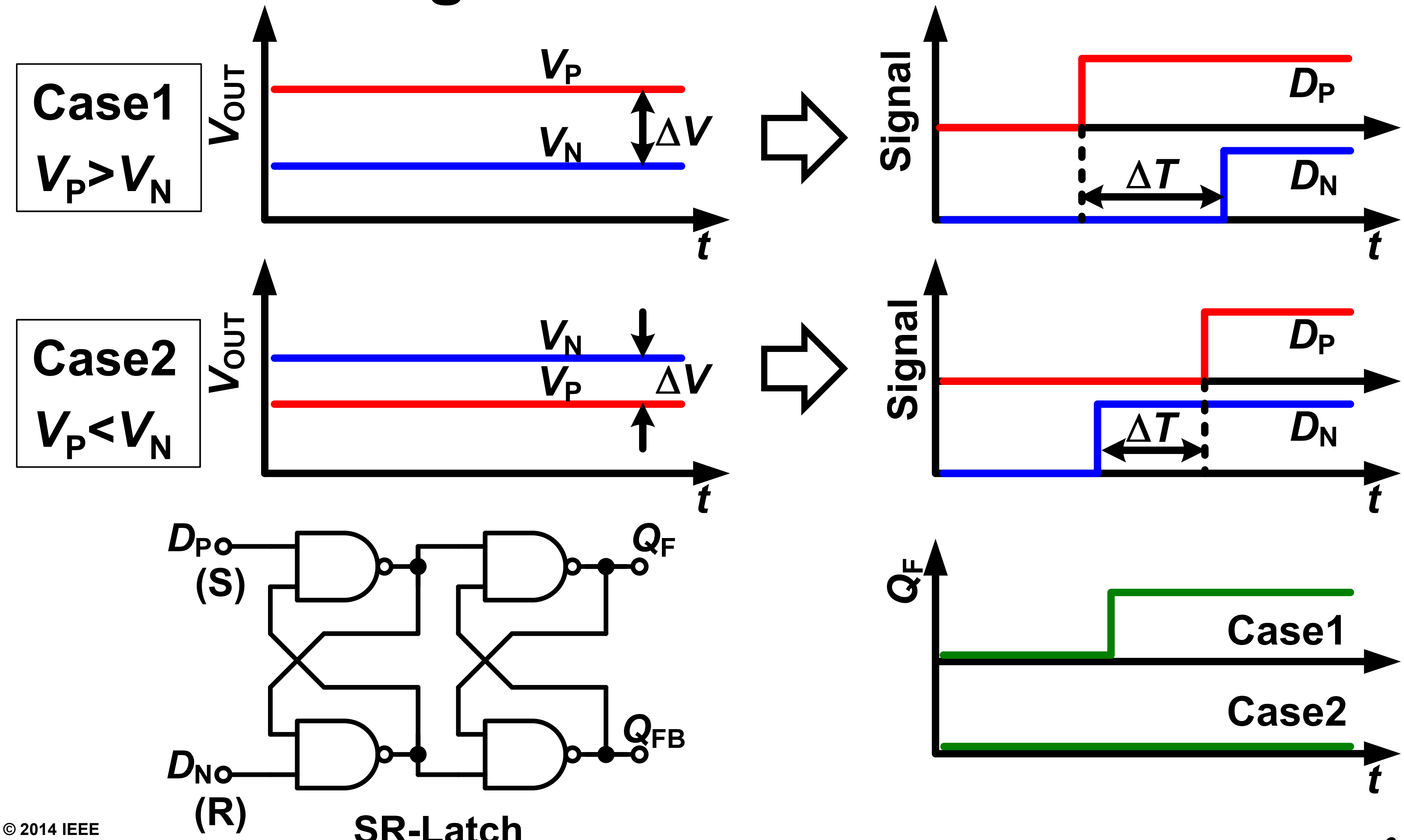
- Voltage-based ⇒ Time-based Folding
  - ☺ More suitable for finer process
- Simple logic circuits can realize folding signal of the timing edge
  - ☺ No static current

Voltage-to-time amplifier

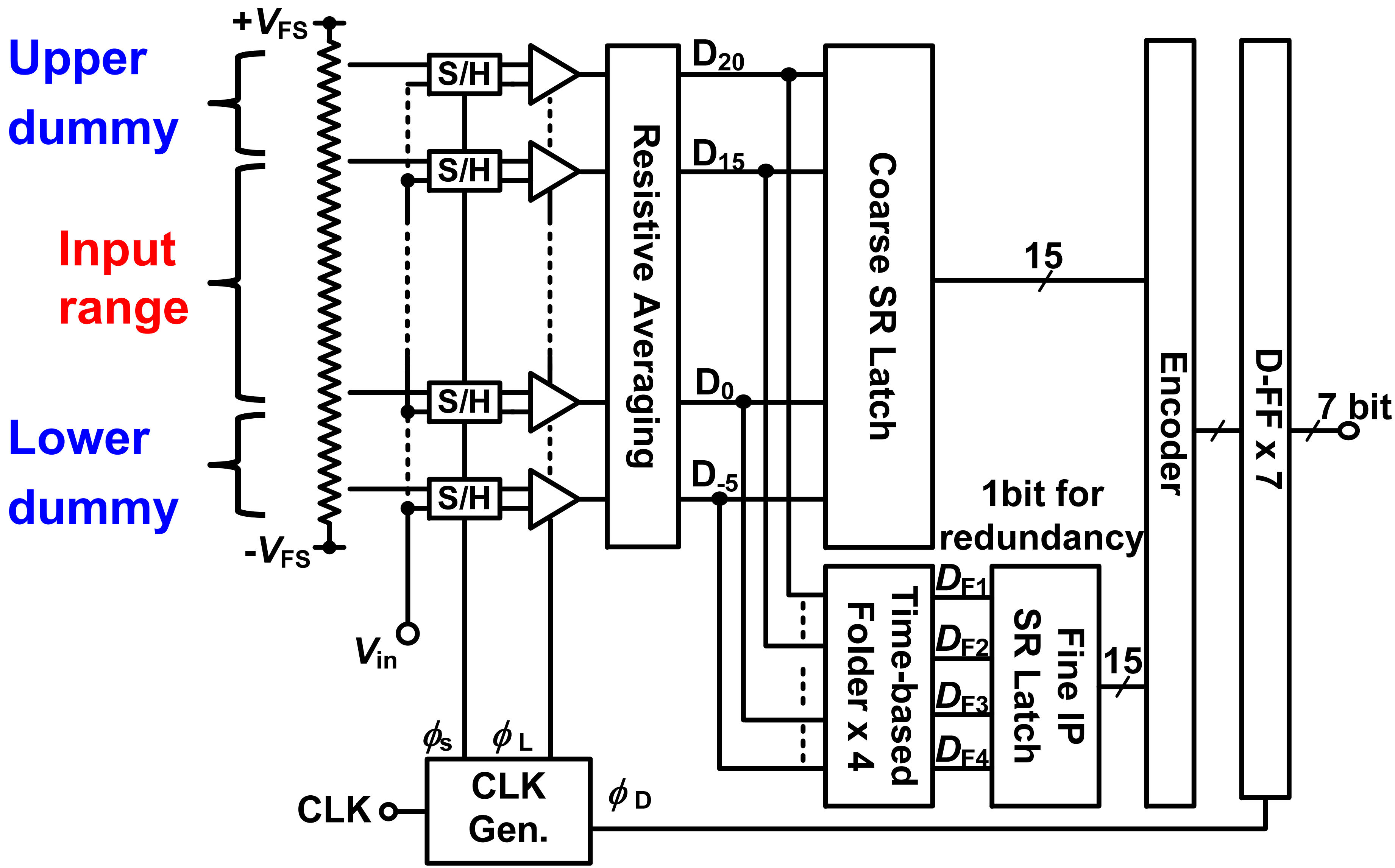
- Dynamic amplifier with resistive averaging
  - ☺ No static current
  - ☺ No need of calibration

Voltage to Time Conversion

Voltage-based | Time-based

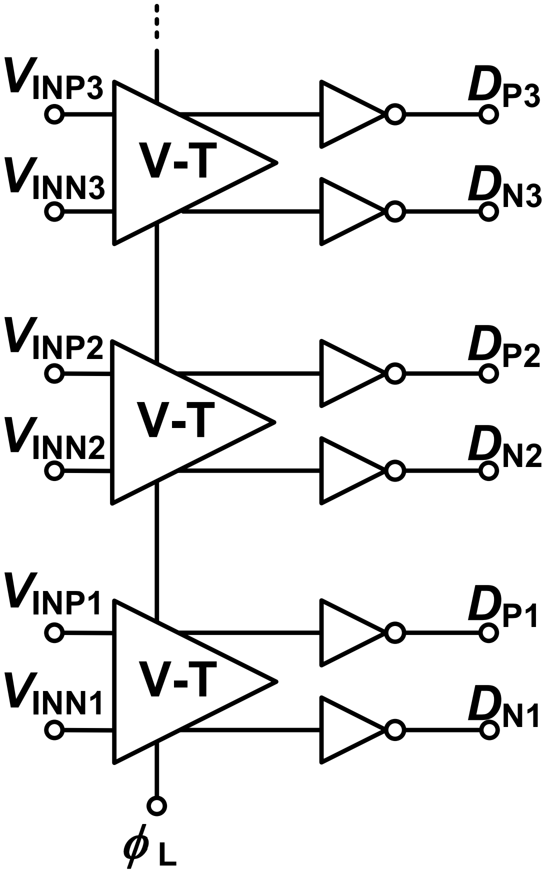


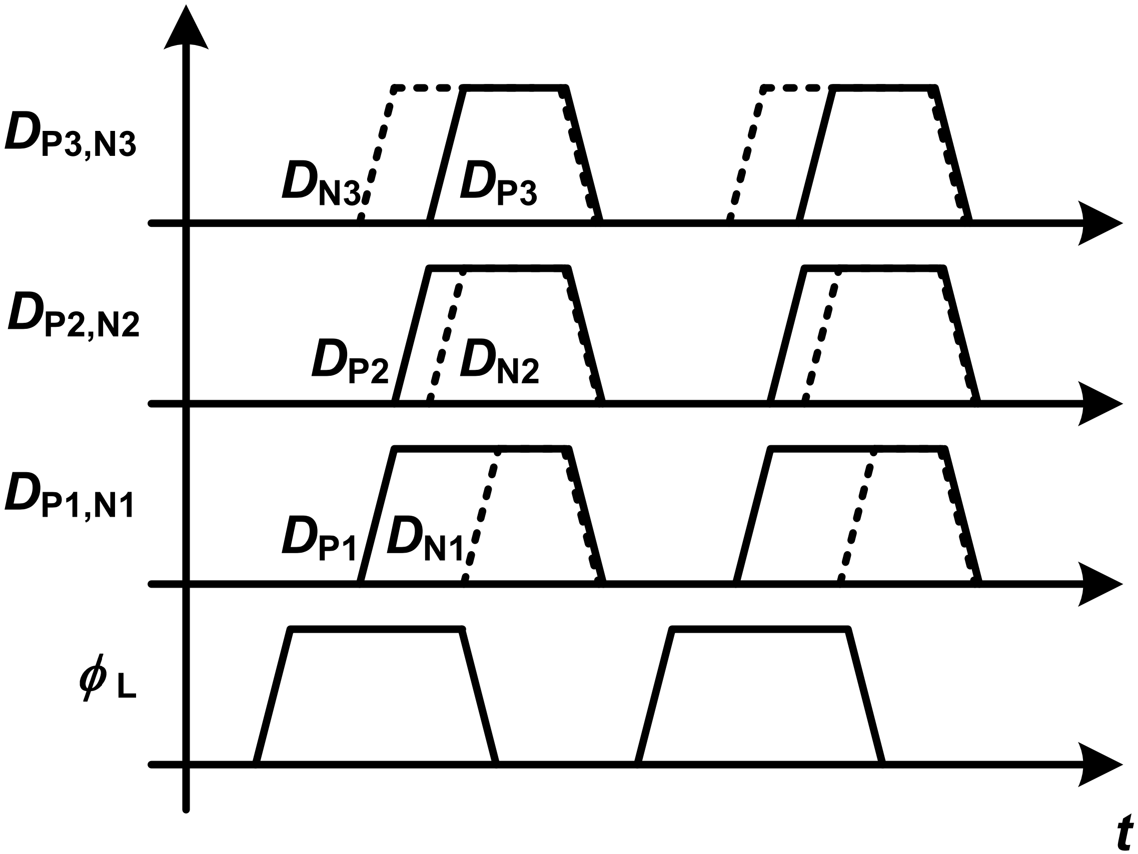
Block Diagram



Output of VT Amps

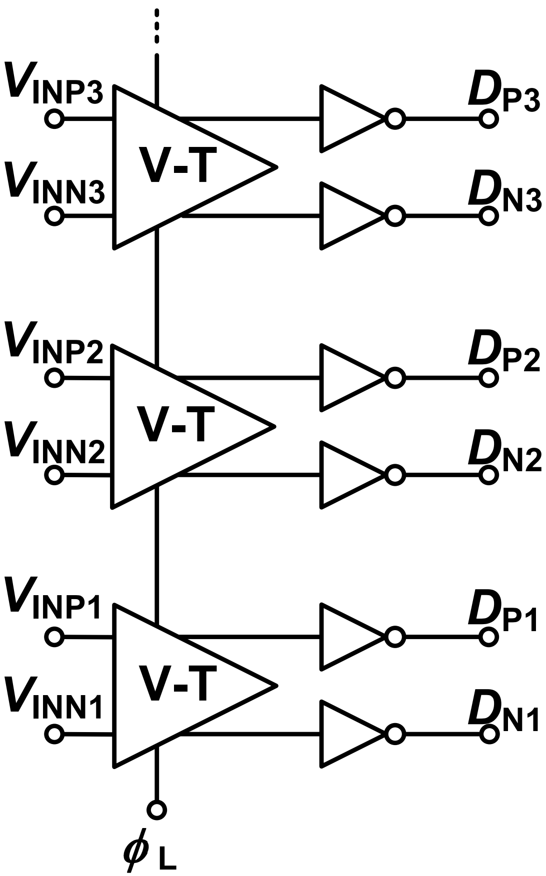
Each VT Amp generates pulse signal which has delay time depending on input signal.

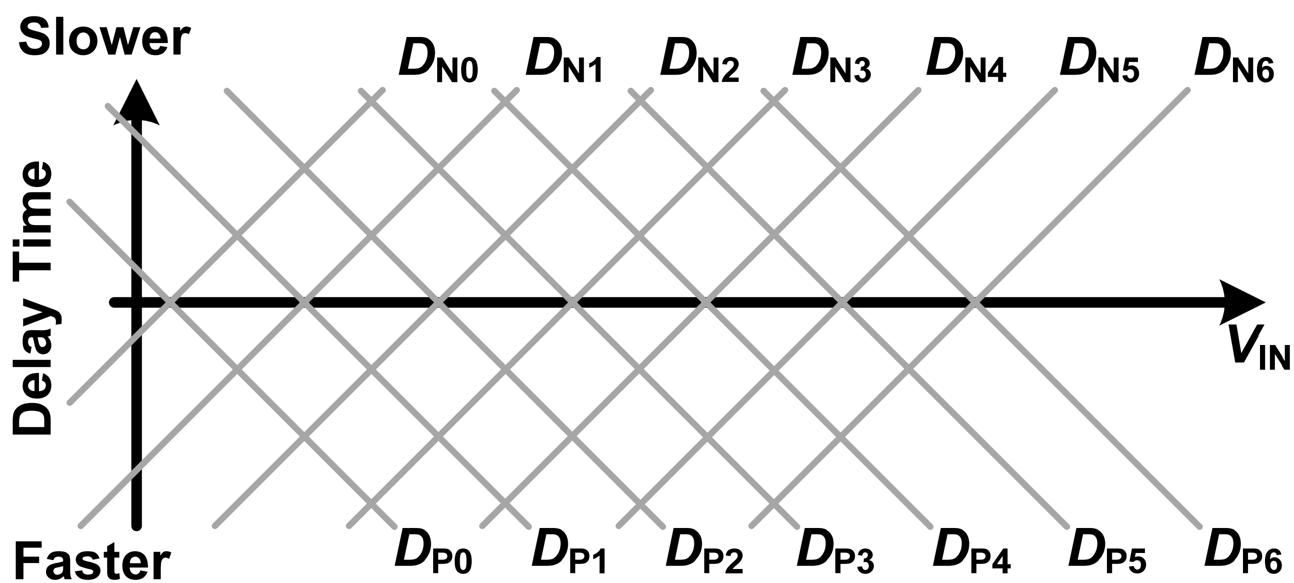




Output of VT Amps

How is the folding signal generated in time domain?

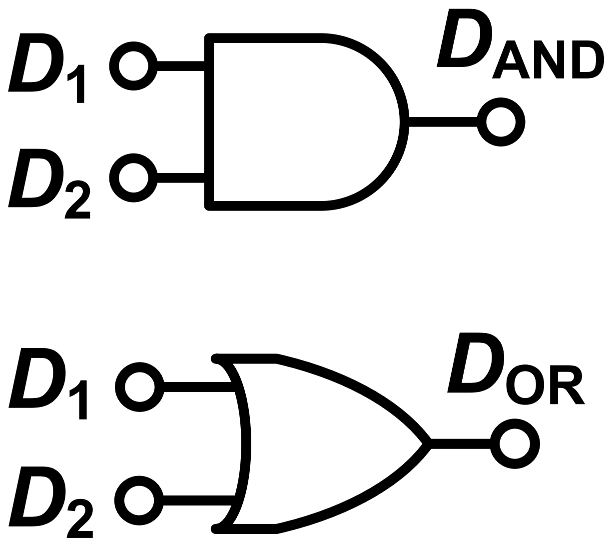




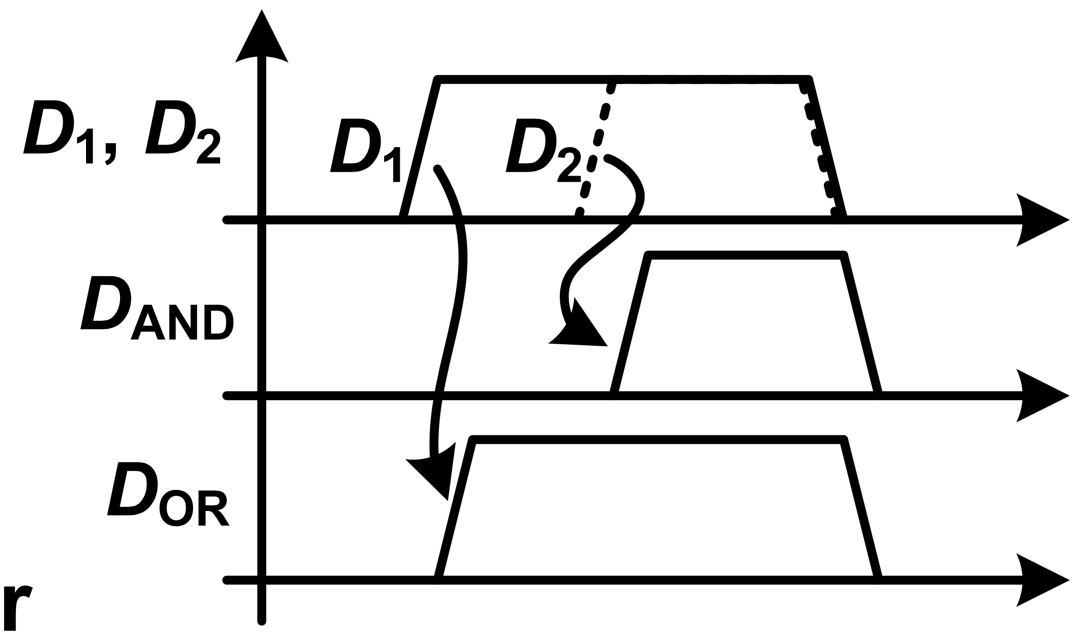
Delay Time Selector

Slower signal ⇒ AND Gate

Faster signal ⇒ OR Gate

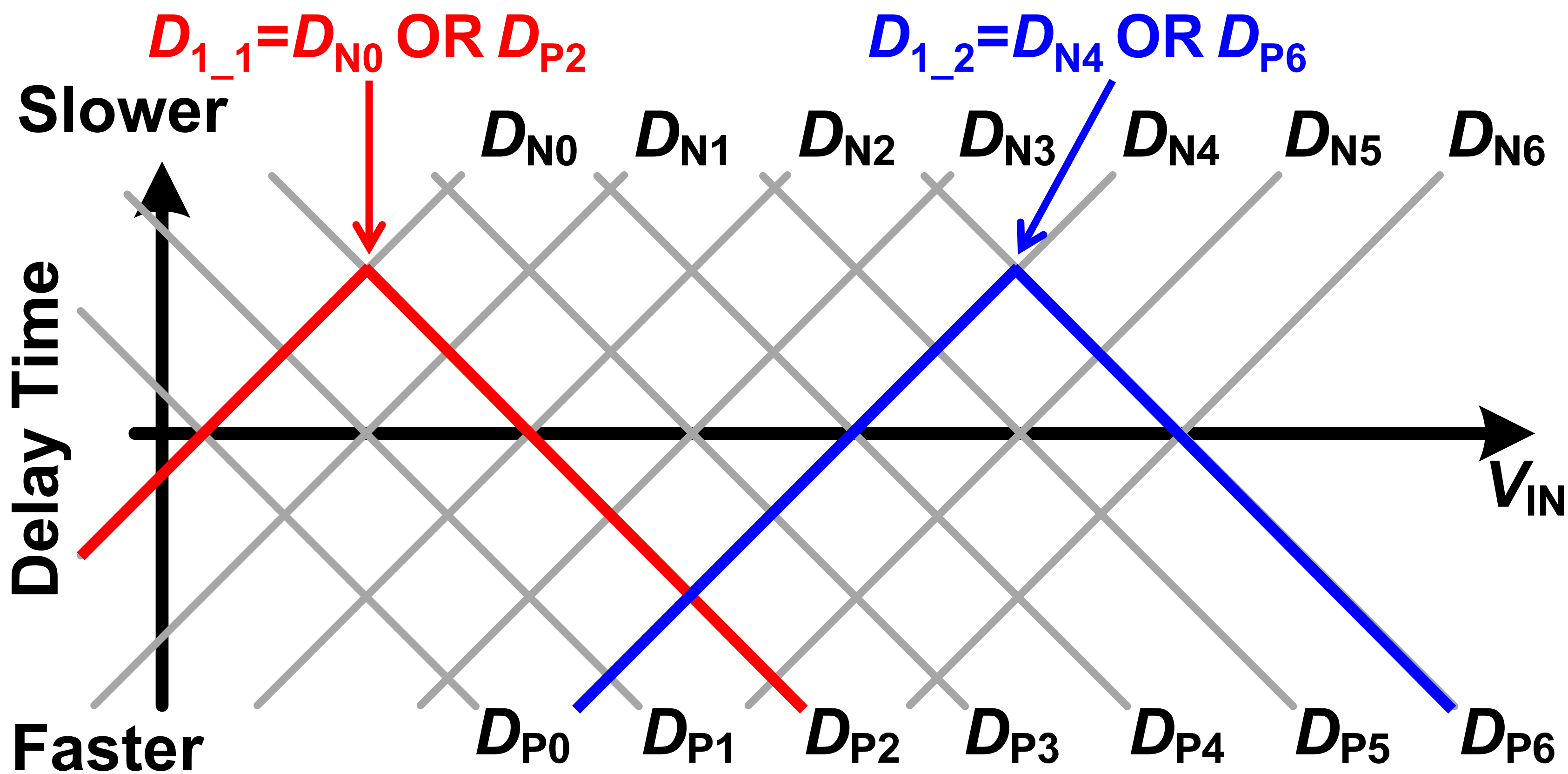


Delay time selector



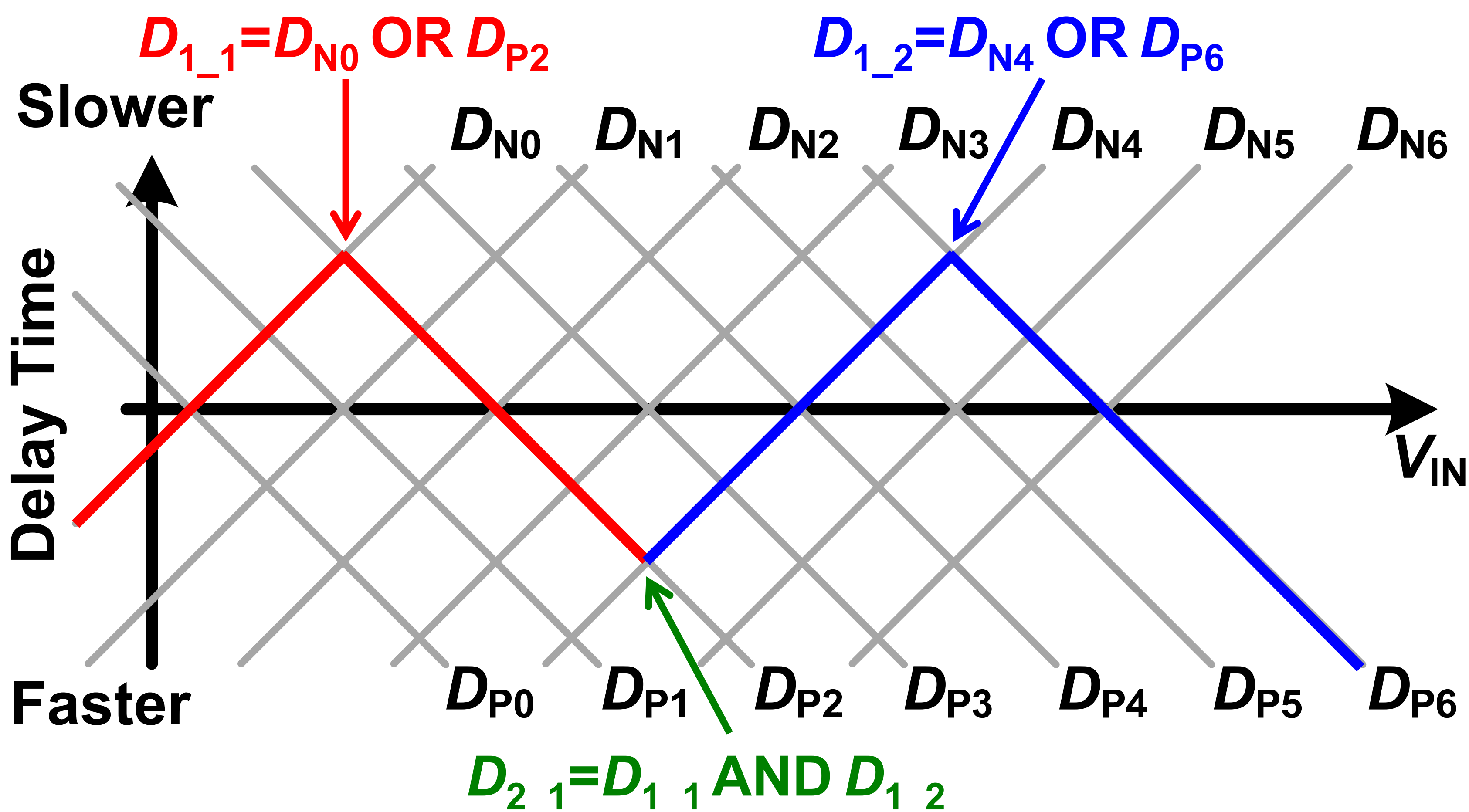
Time-Based-Folding

Peak fold ⇒ OR gate



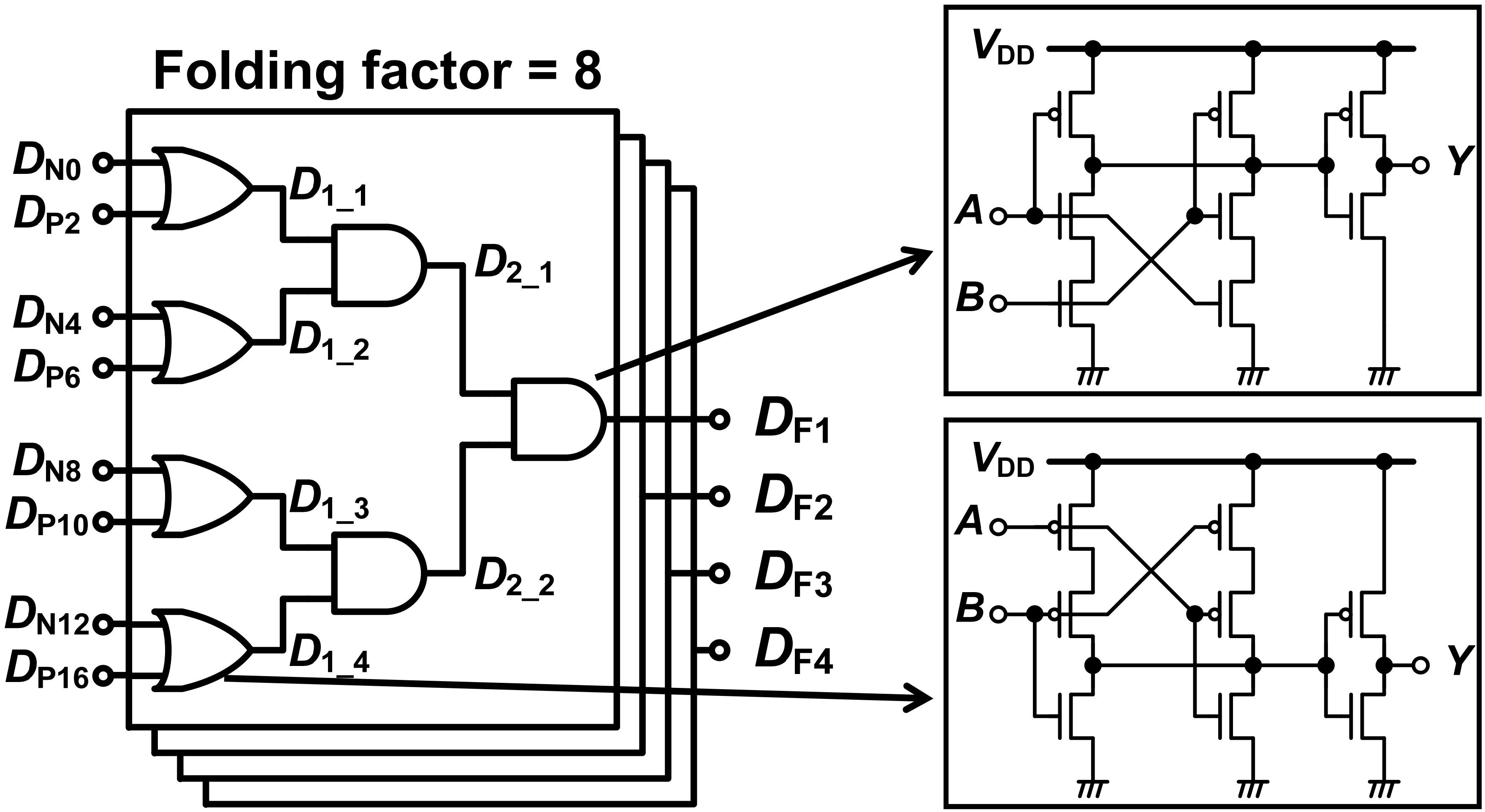
Time-Based-Folding

Valley fold ⇒ AND gate



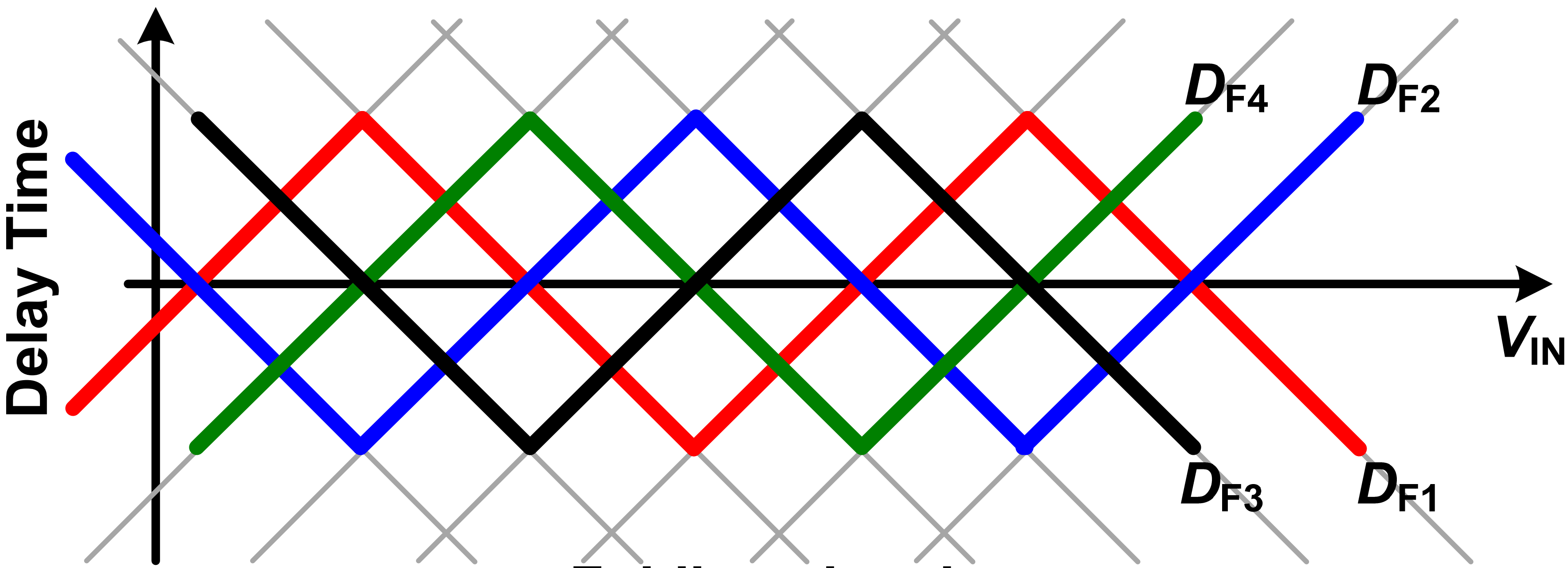
TF Circuit Implementation

Symmetrical input logic cells are used for realizing same transition time.



TF output for interpolation

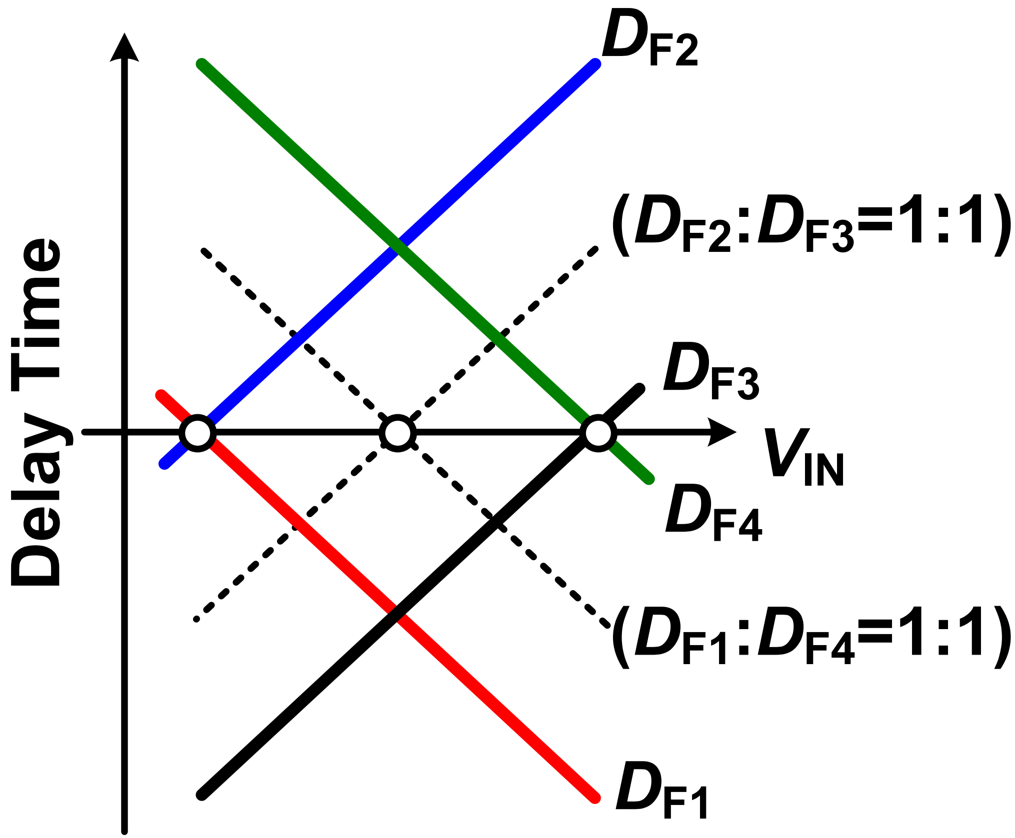
Time-based folder outputs four signals to interpolate in the fine SR latches.



Folding signals

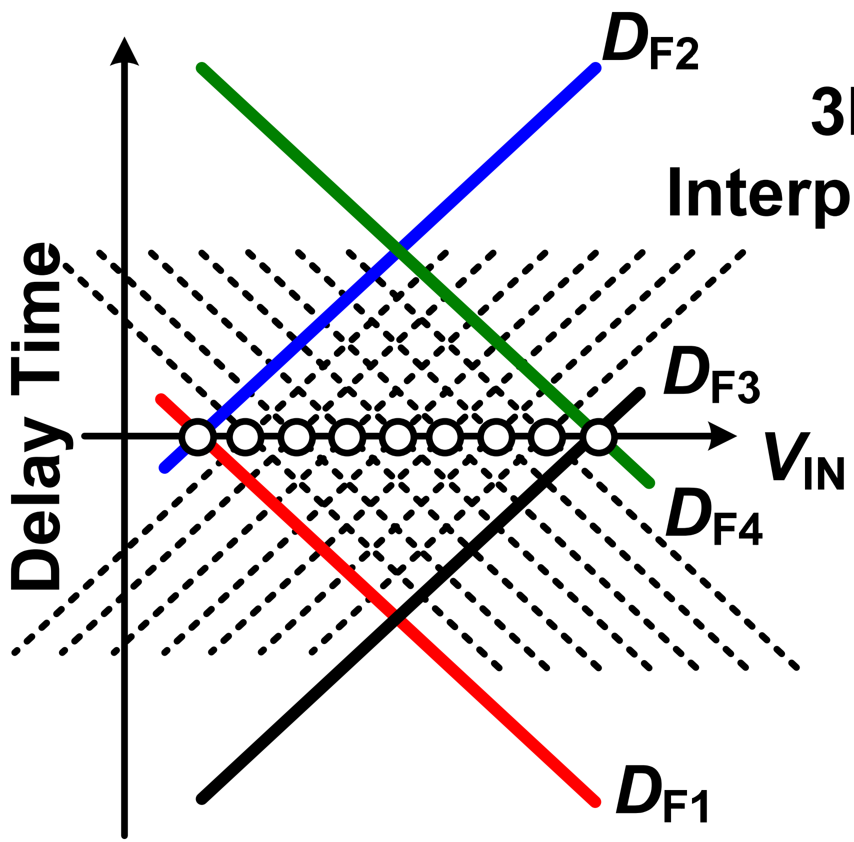
TF output for interpolation

Time-based folder outputs four signals to interpolate in the fine SR latches.



TF output for interpolation

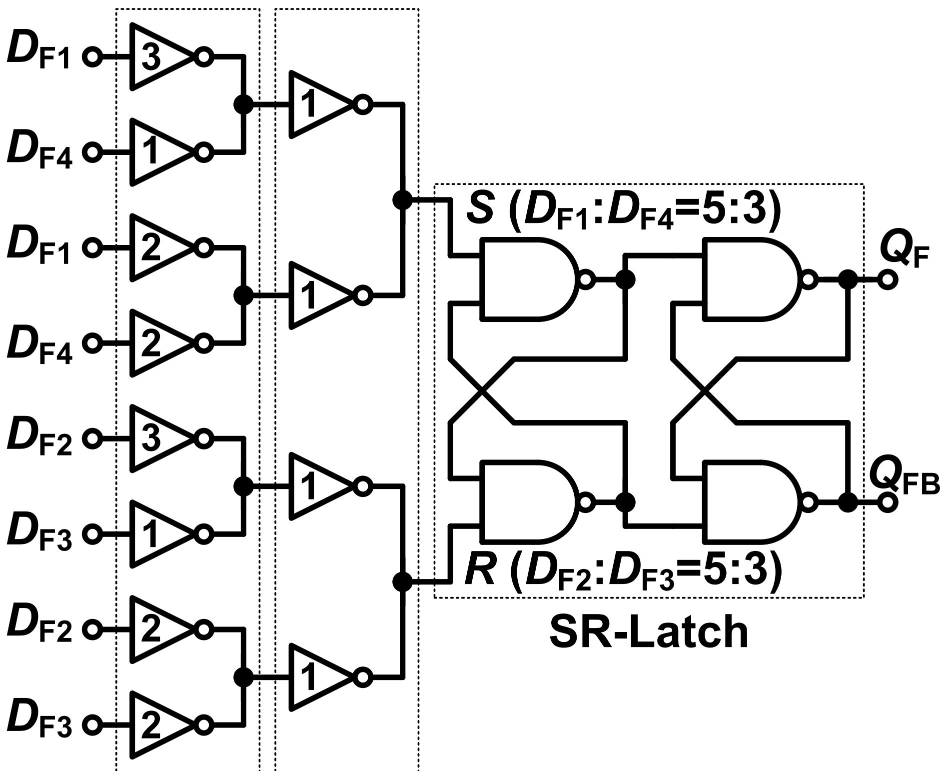
Time-based folder outputs four signals to interpolate in the fine SR latches.

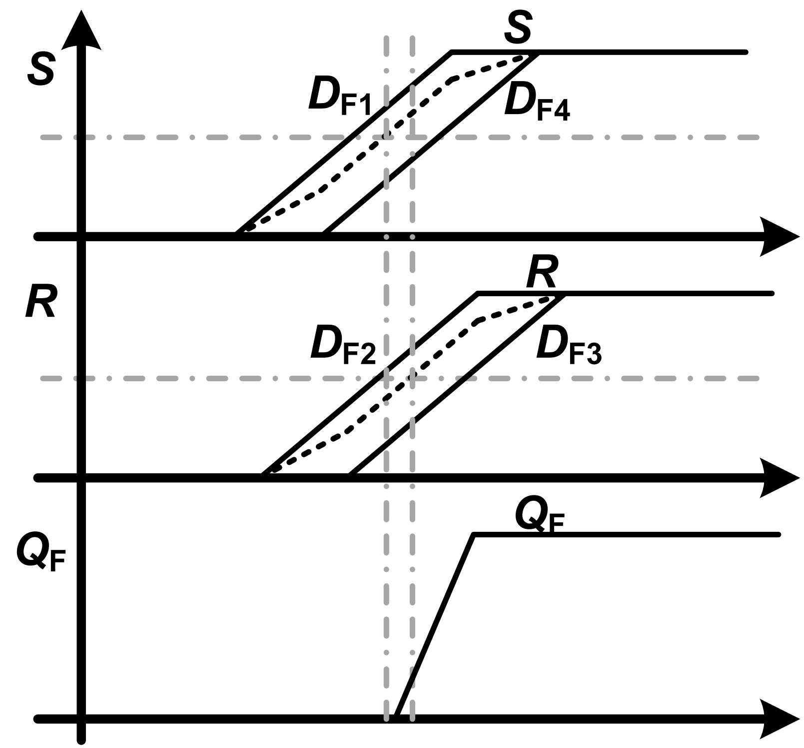


Interpolated SR Latch

Gate weighted inverter realizes interpolated signal [6]

⇒No need of reference signal in fine SR latches.





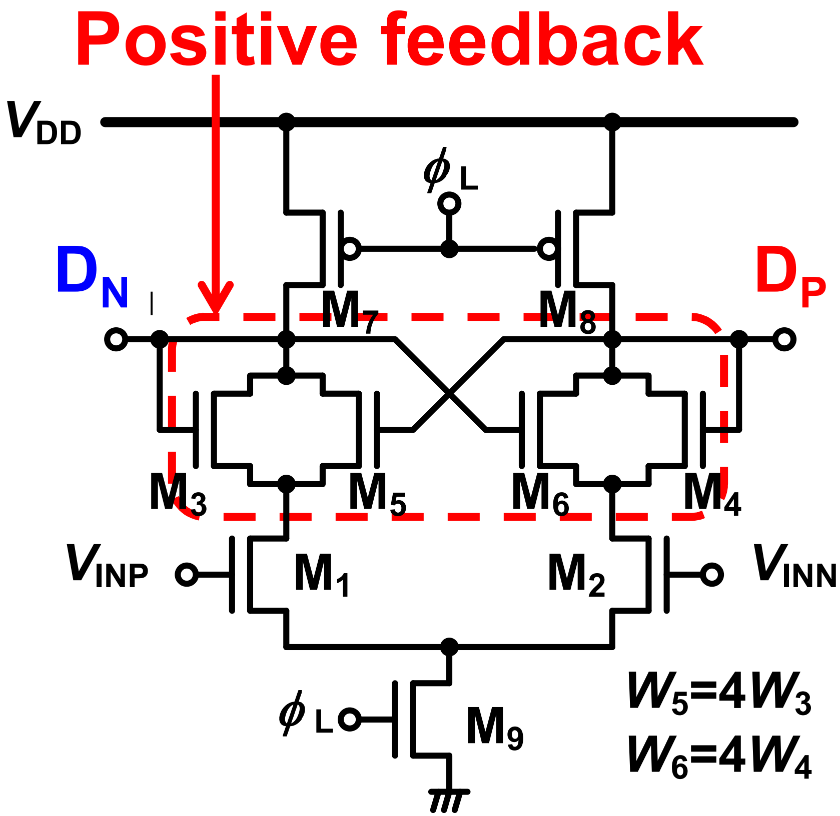
SR-Latch response in the case of interpolation ratio of 5:3

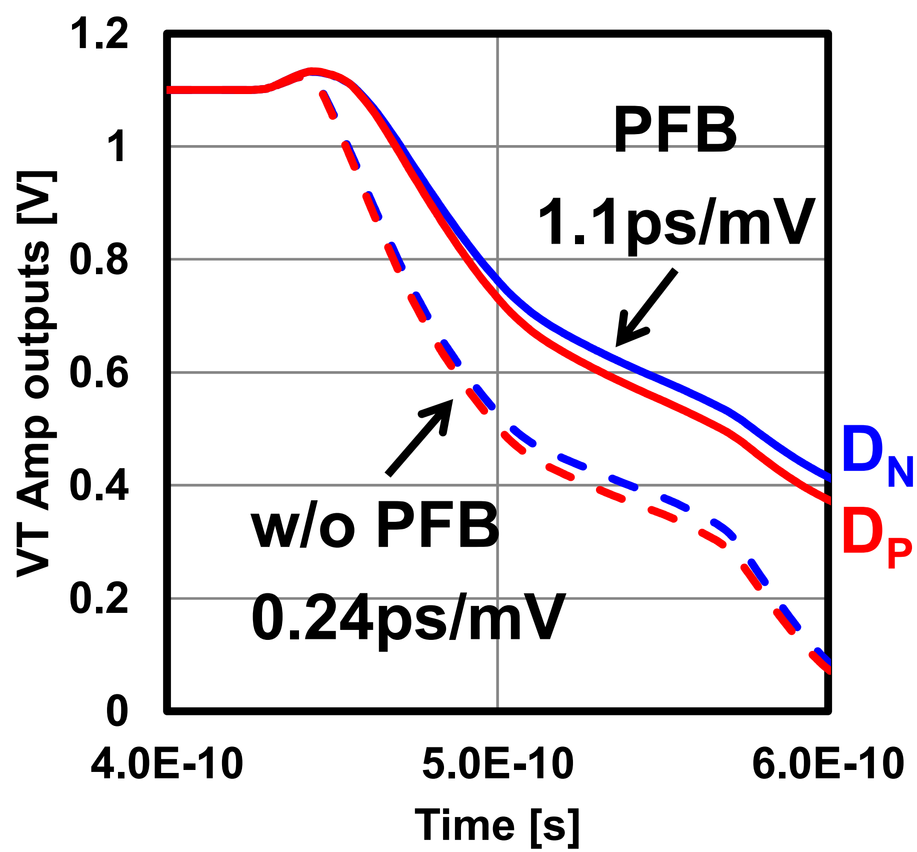
[6] D. Miyashita, *et al.*, VLSI symp. 2011

Voltage-to-Time Amplifier

PFB can increase the gain by about 4 times.

⇒No need calibration in coarse and fine Latches.

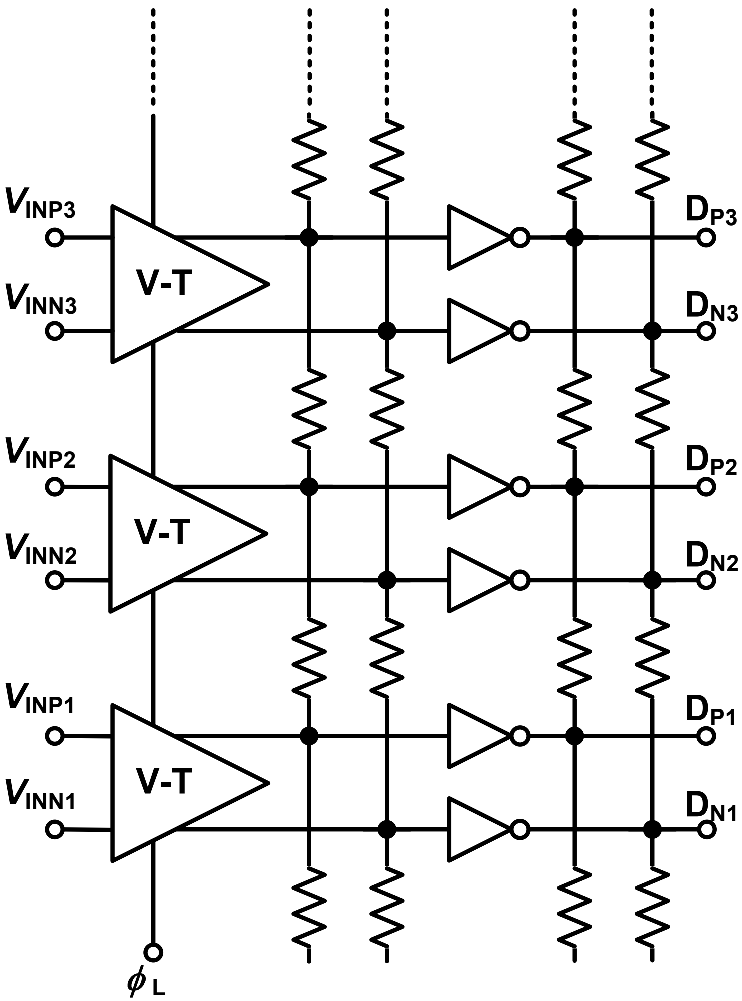


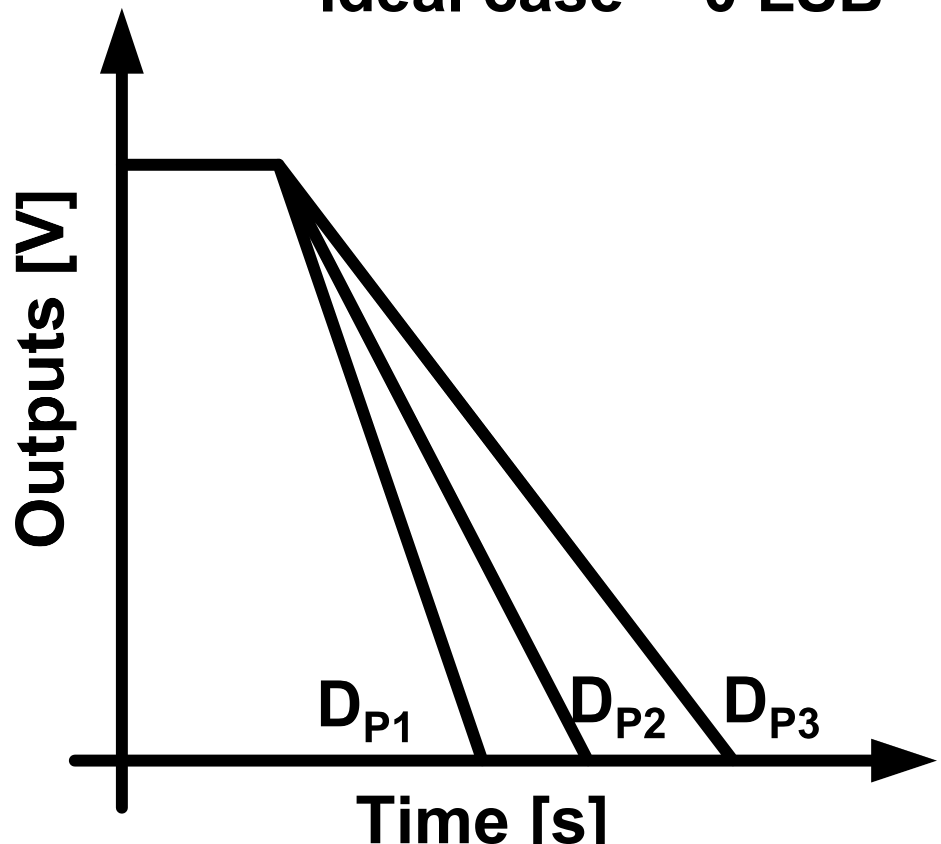


Resistively Averaged VT Amps

Resistive averaging reduces the mismatch voltage.

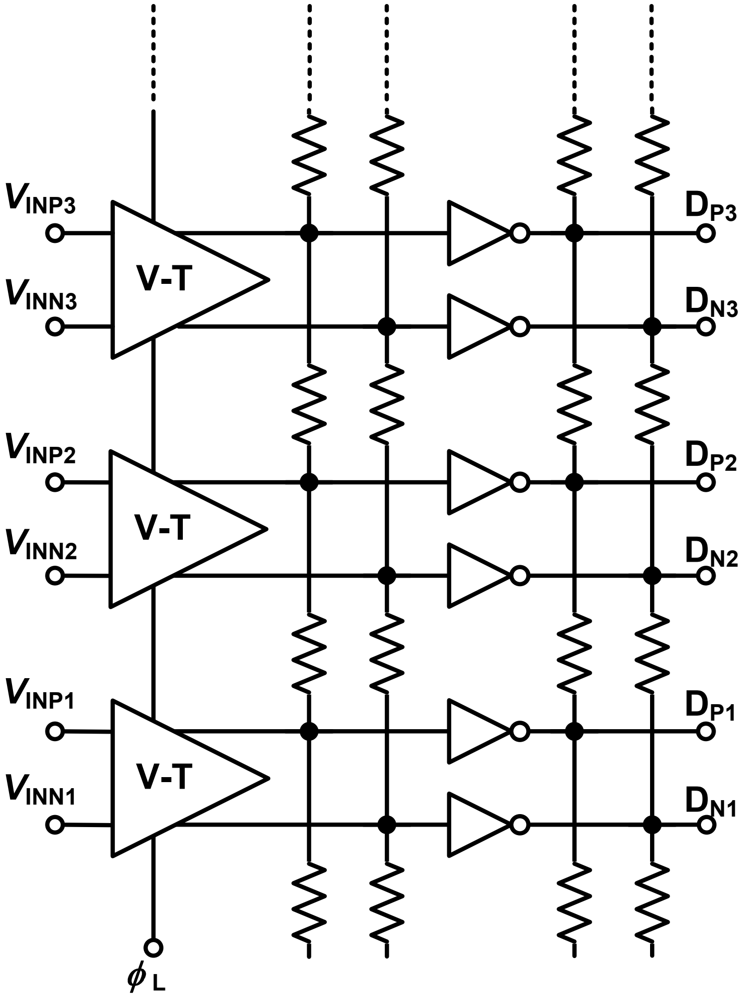
	DNL(σ)
Ideal case	0 LSB



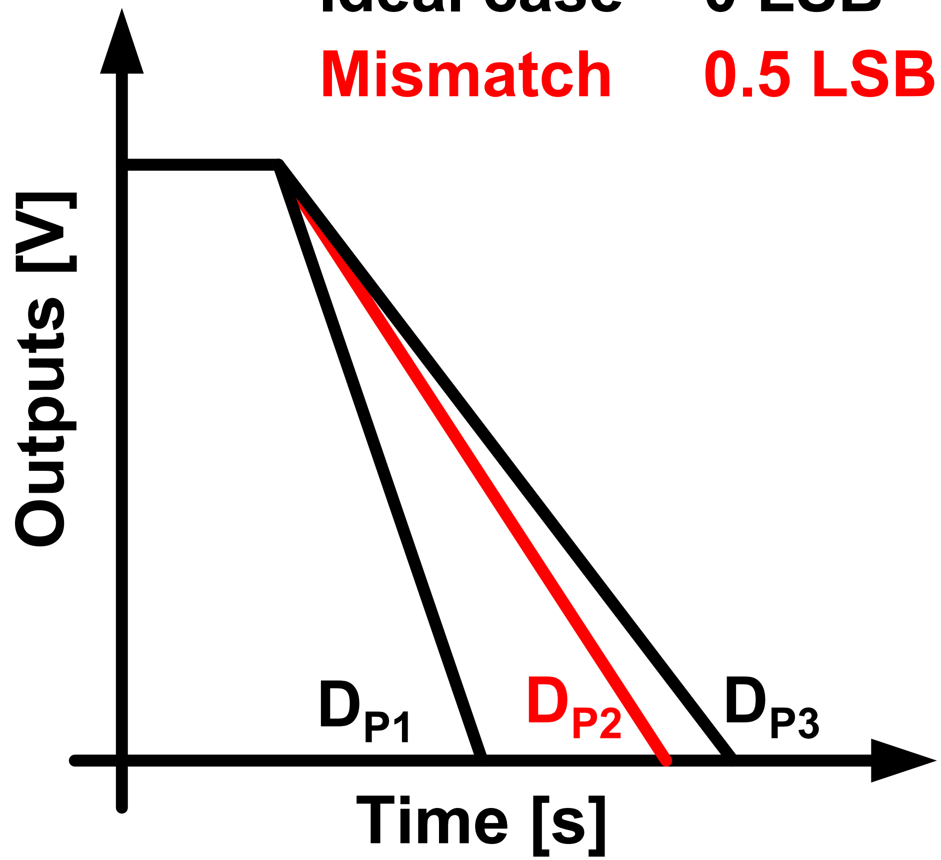


Resistively Averaged VT Amps

Resistive averaging reduces the mismatch voltage.

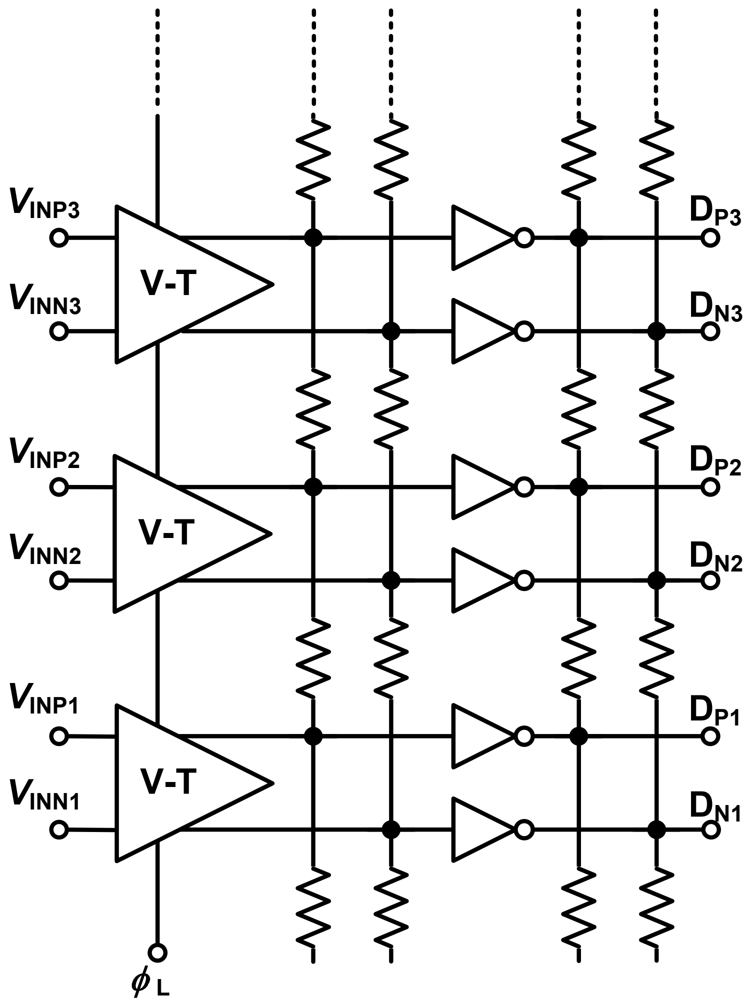


	DNL(σ)
Ideal case	0 LSB
Mismatch	0.5 LSB

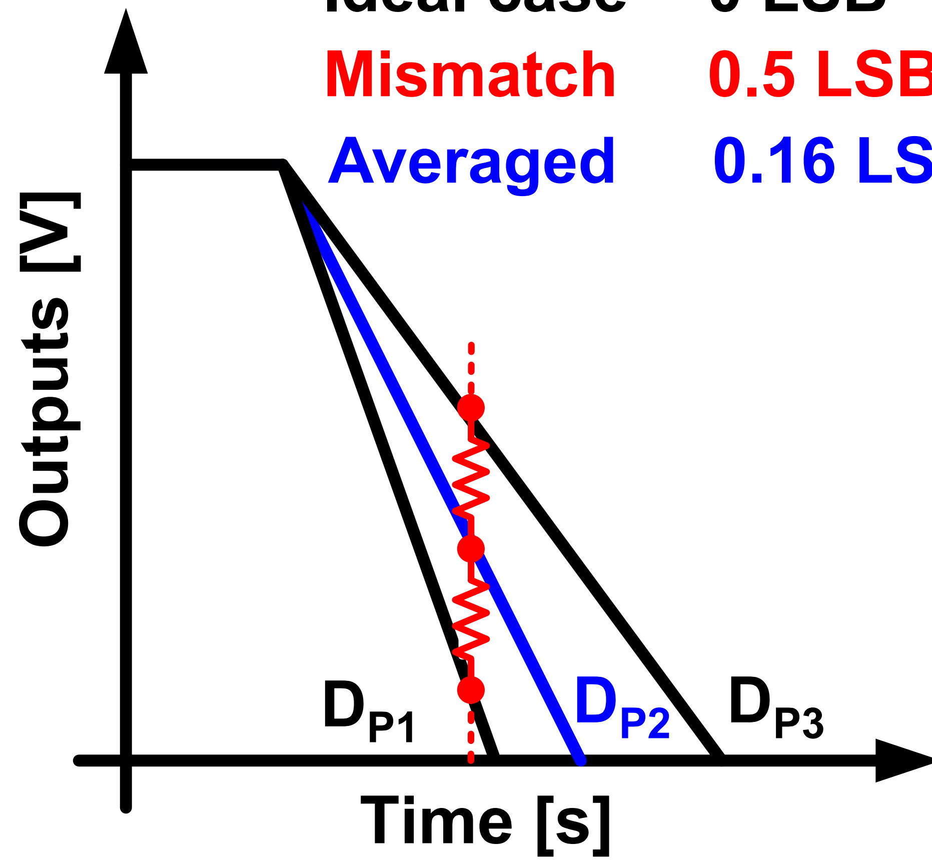


Resistively Averaged VT Amps

Resistive averaging reduces the mismatch voltage.

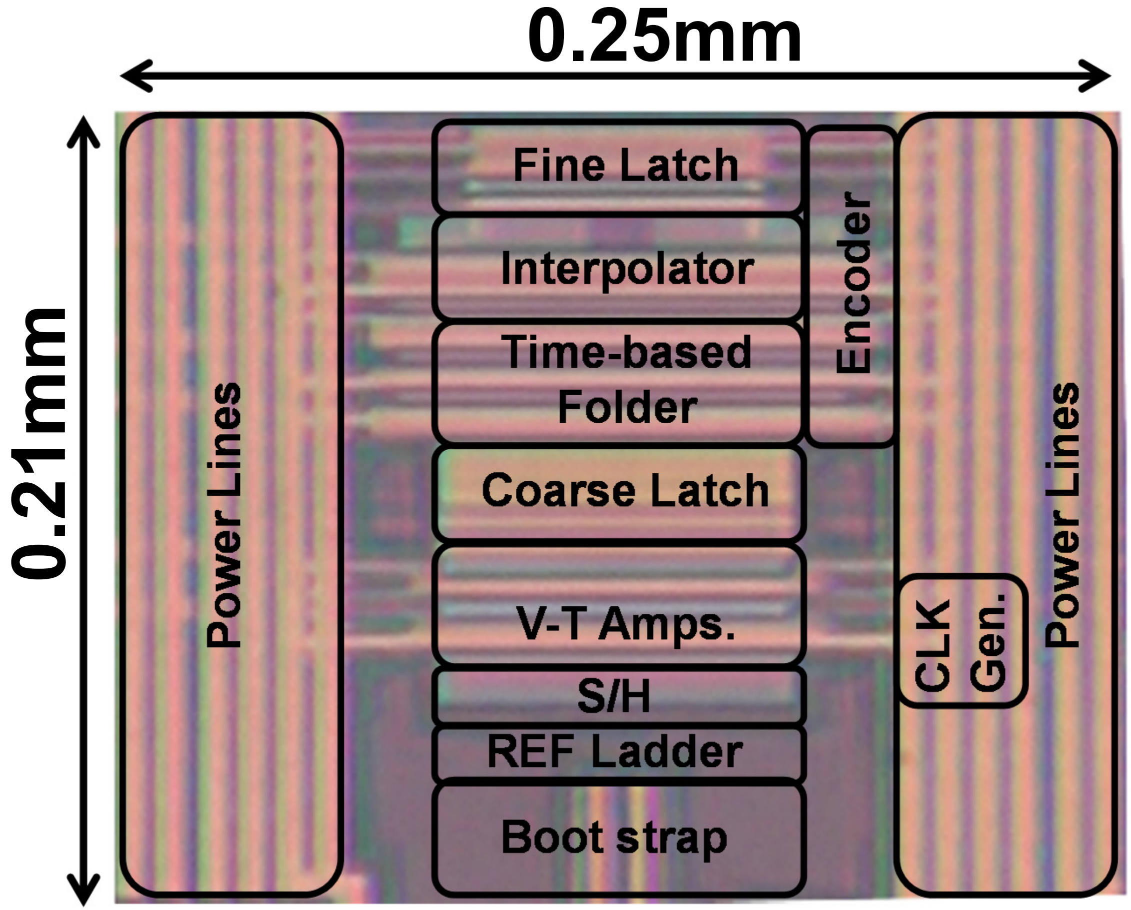


	DNL(σ)
Ideal case	0 LSB
Mismatch	0.5 LSB
Averaged	0.16 LSB

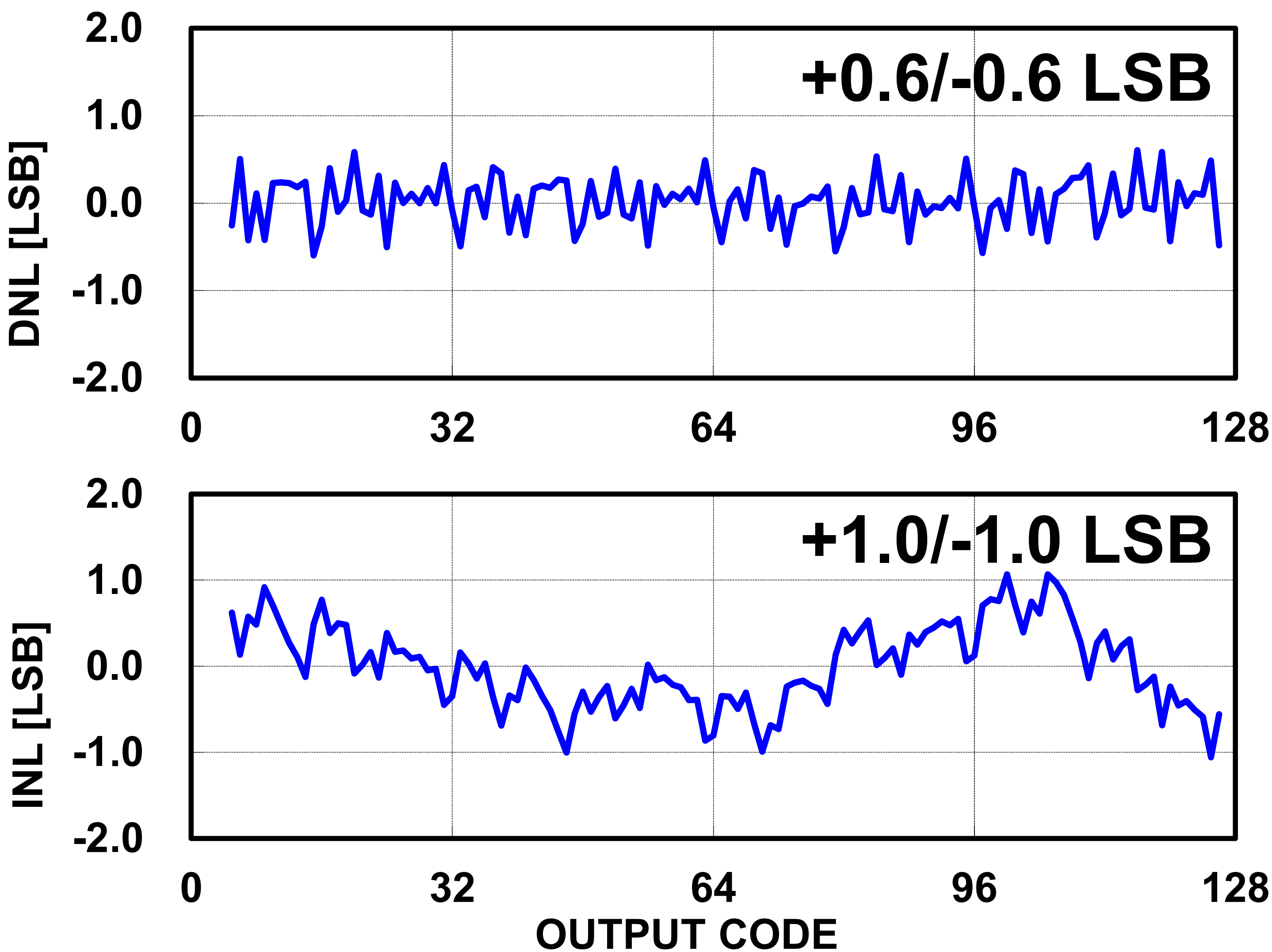


Chip photo

- 40nm LP 8M1P CMOS technology
- Chip area of 0.052mm^2



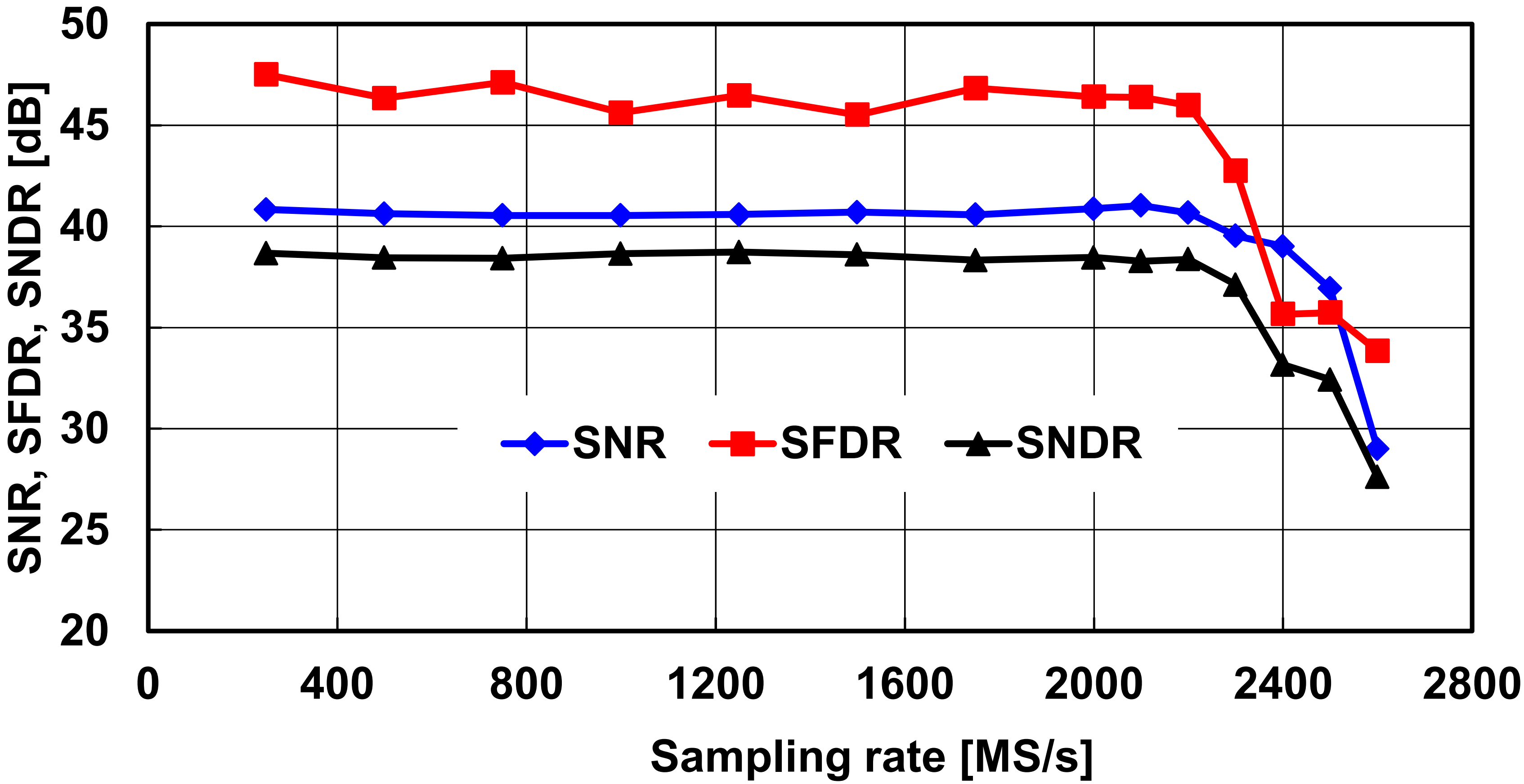
Measured DNL, INL



Sampling rate vs. SNDR

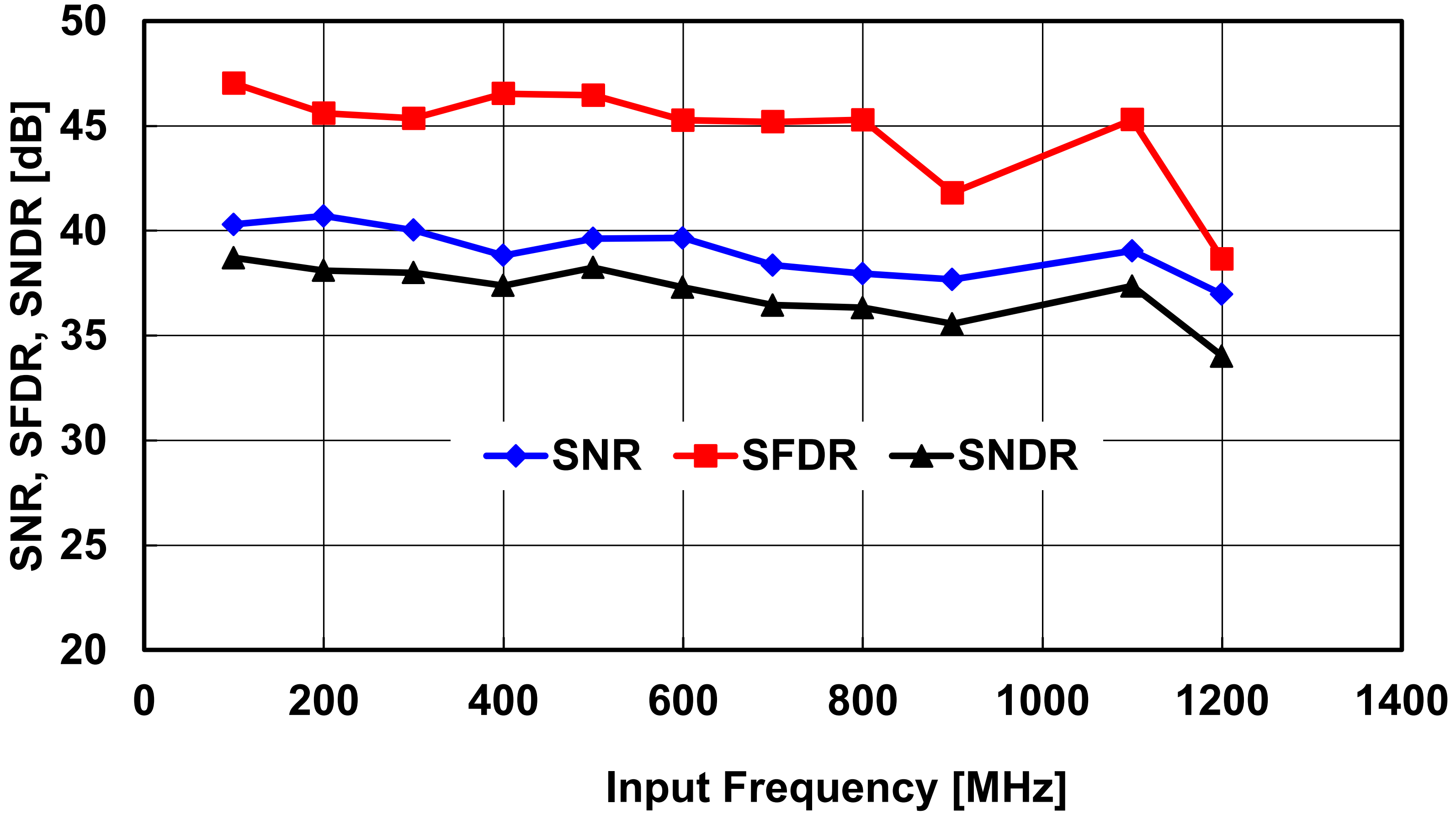
Input Frequency = 100MHz

SNDR =38.3dB@2.2GS/s



Input Frequency vs. SNDR

Sampling rate = 2.2GS/s
SNDR =37.4dB@1.1GHz

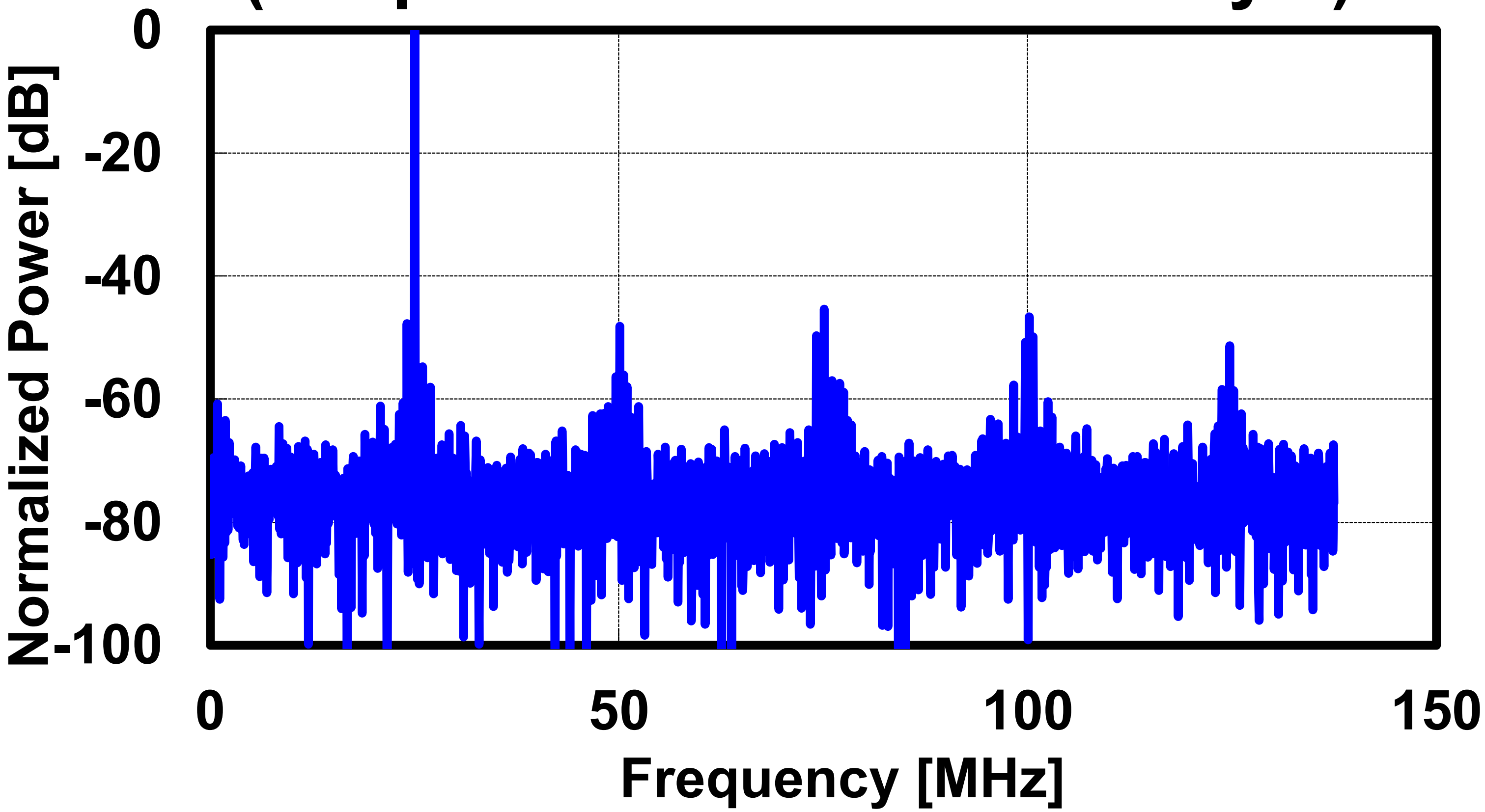


Measured Spectrum

Sampling rate = 2.2GS/s

Input frequency = 800MHz

(Output code is decimated by 8)



Performance Summary

- The highest SNDR in Flash ADCs exceeding 2 GS/s
- No need of calibration

	ISSCC 2008 [3]	VLSI 2012 [8]	VLSI 2013 [9]	This work
Technology	90nm	40nm	32nm SOI	40nm LP
Resolution [bit]	5	6	6	7
Power Supply [V]	1	1.1	0.85	1.1
Sampling Frequency [GS/s]	1.75	3	5	2.2
Power Consumption [mW]	2.2	11	8.5	27.4
SNDR @Nyquist [dB]	27.6	33.1	30.9	37.4*
FoMw [fJ/conv.-step]	64.5	99.3	59.4	210
FoMs [dB]	143.5	144.4	145.6	143.3
Core area [mm^2]	0.0165	0.021	0.02	0.052
Calibration	Off chip	Foreground	Off chip	No need

*3.3mW for reference ladder, 19.4mW for analog and 4.7mW for digital

Conclusion

- **Time-based-folding architecture**
  - ☺ More suitable for future process
  - ☺ No static current
- **Voltage-to-time amplifier**
  - •Dynamic amplifier with resistive averaging
    - ☺ No static current
    - ☺ 1/3 offset voltage, no need of calibration
- **A 7b 2.2GS/s 27.4mW Folding Flash ADC is realized**

Acknowledgement

This work was partially supported by MIC, Berkeley Design Automation for the use of the Analog Fast SPICE(AFS) Platform, and VDEC in collaboration with Cadence Design Systems, Inc.

References

[1] Y. Nakajima, *et al*., "A Background Self-Calibrated 6b 2.7GS/s ADC With Cascade-Calibrated Folding-Interpolating Architecture," *IEEE J. Solid-State Circuits*, vol. 45, pp. 707-718, Apr. 2010.

[2] T. Yamase, *et al*., "A 22-mW 7b 1.3-GS/s Pipeline ADC with 1-bit/stage Folding Converter Architecture," *Symp. VLSI Circuits*, pp. 124-125, June 2011.

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A 14b 4.6GS/s RF DAC in 0.18μm CMOS for Cable Head-End Systems

Brian Brandt, Dan McMahill, Miaochen Wu, Paul Kalthoff, Ajay Kuckreja, Geir Ostrem

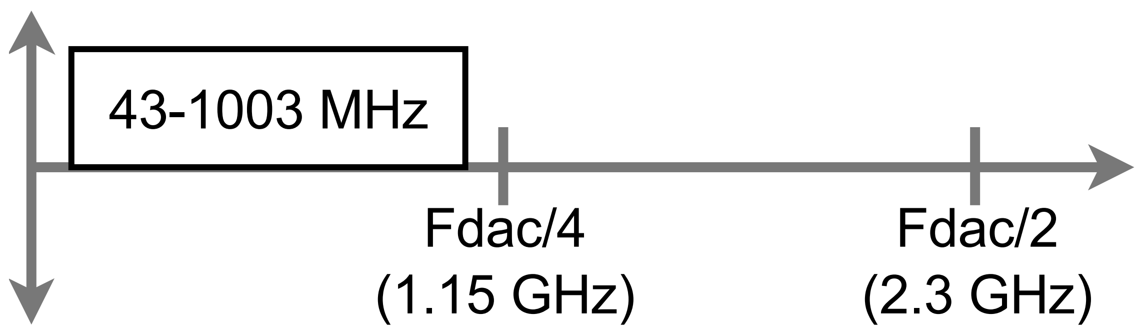
Maxim Integrated

Outline

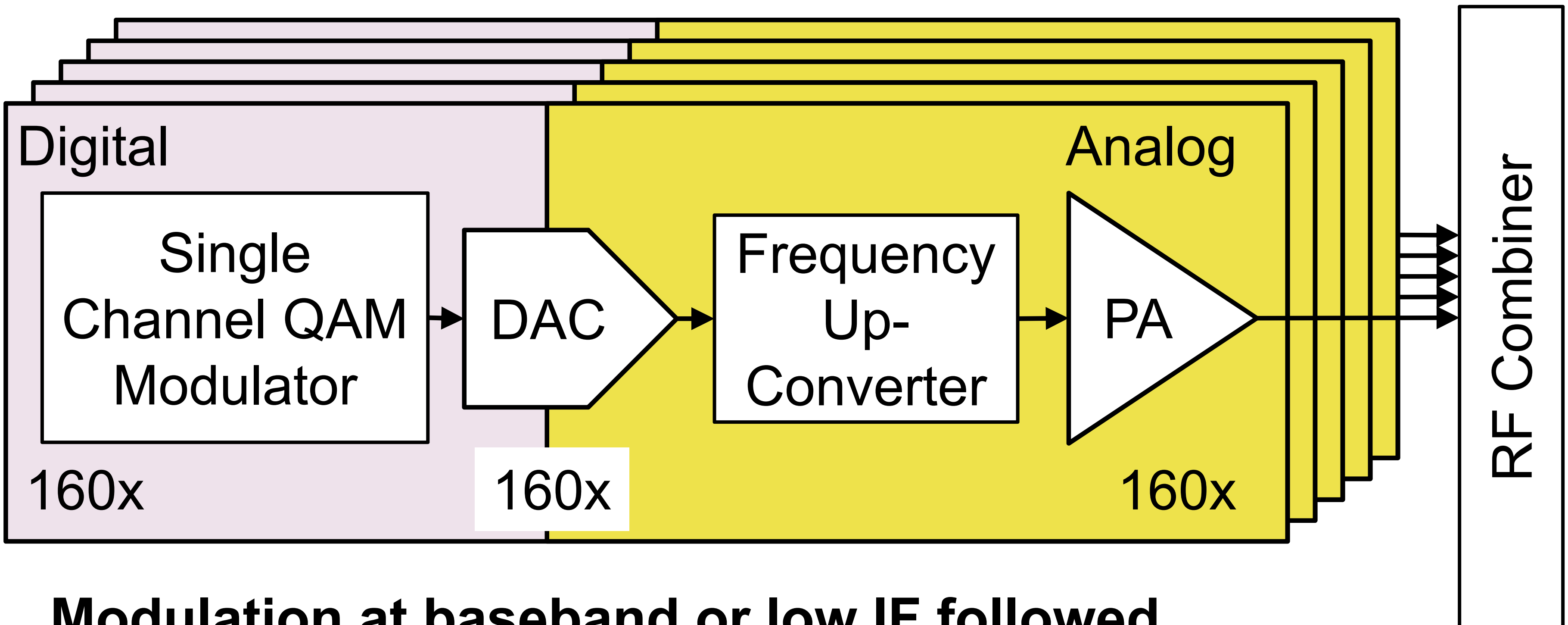
- CATV Downstream Architecture/Motivation
- DAC Architecture/Circuit Details
- Digital Predistortion (DPD)
- Experimental Results
- Summary

System Requirements

- Output bandwidth is 43-1003 MHz
- Spurious and noise within 43-1003 MHz < -73 dBc for a single QAM with adjustments made for multiple carriers
- 6 MHz/channel, up to 160 channels (960 MHz total)

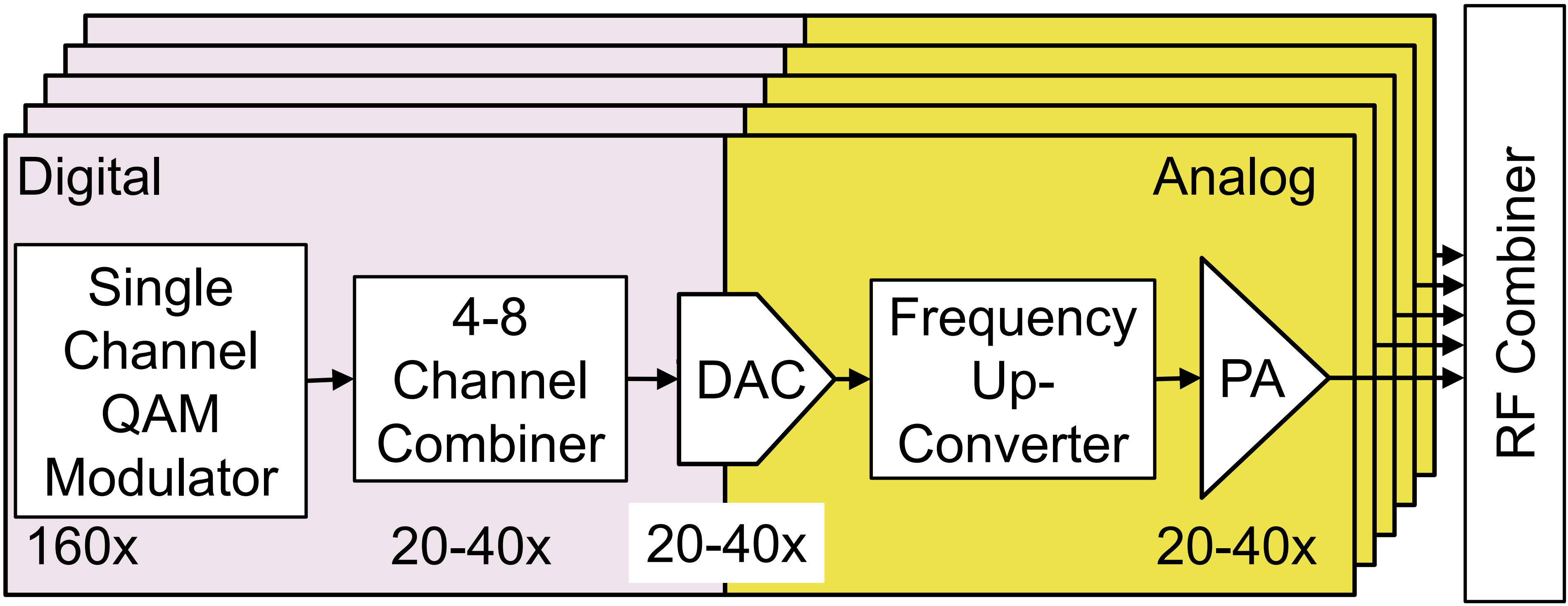


Evolution of QAM Modulators for CATV



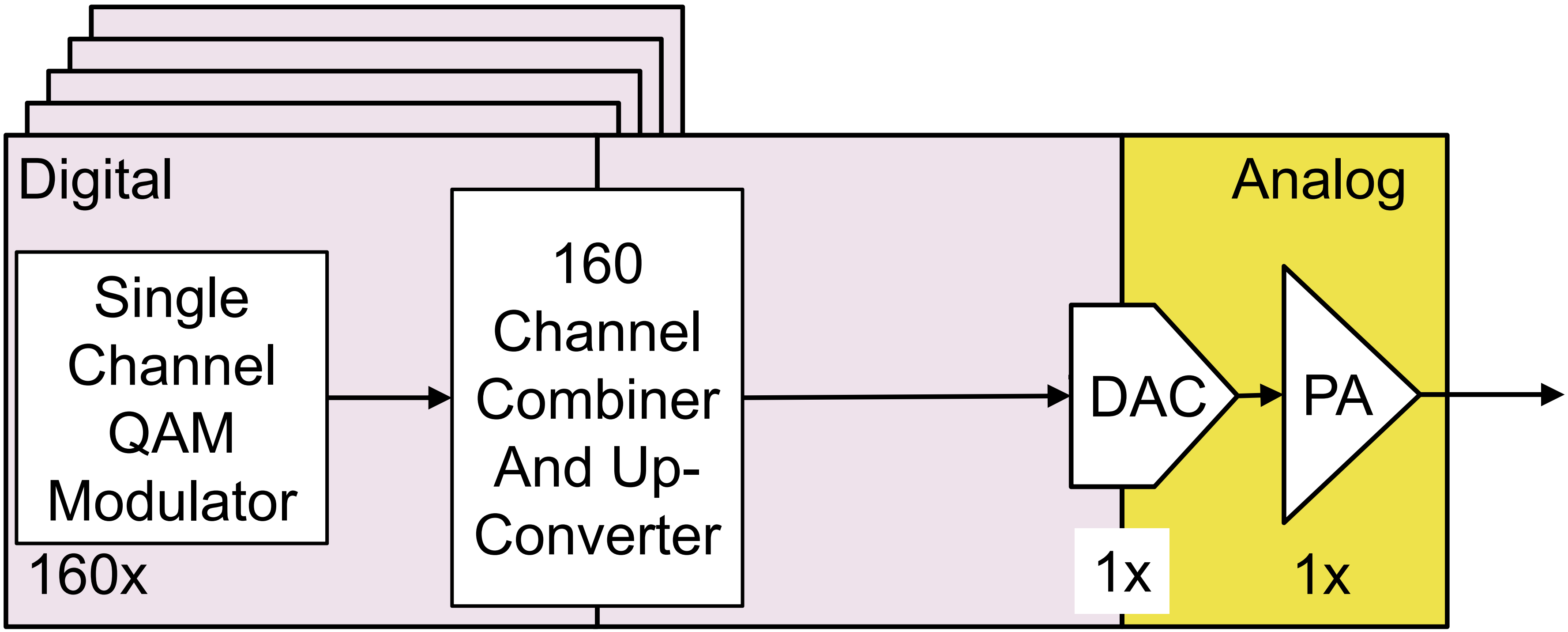
Modulation at baseband or low IF followed by analog/RF frequency up-conversion. One complete signal chain per channel.

Evolution of QAM Modulators for CATV



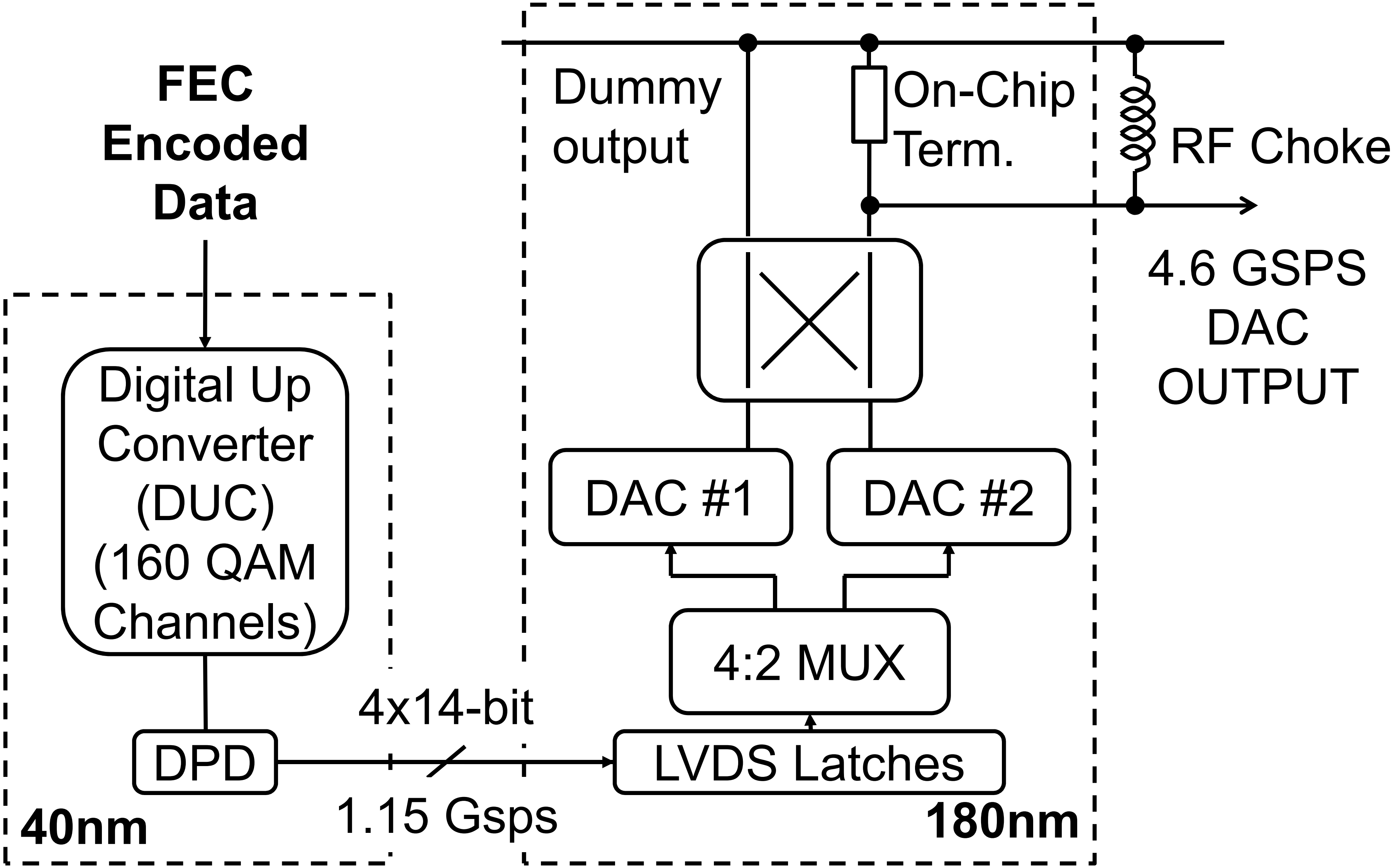
Multiple (4-8) QAM per signal chain with analog/RF frequency up-conversion. One complete signal chain for every 4-8 channels.

Evolution of QAM Modulators for CATV



Direct Bits to RF:
- No Analog/RF frequency converters
- Single PA for all channels
- Single DAC for all channels

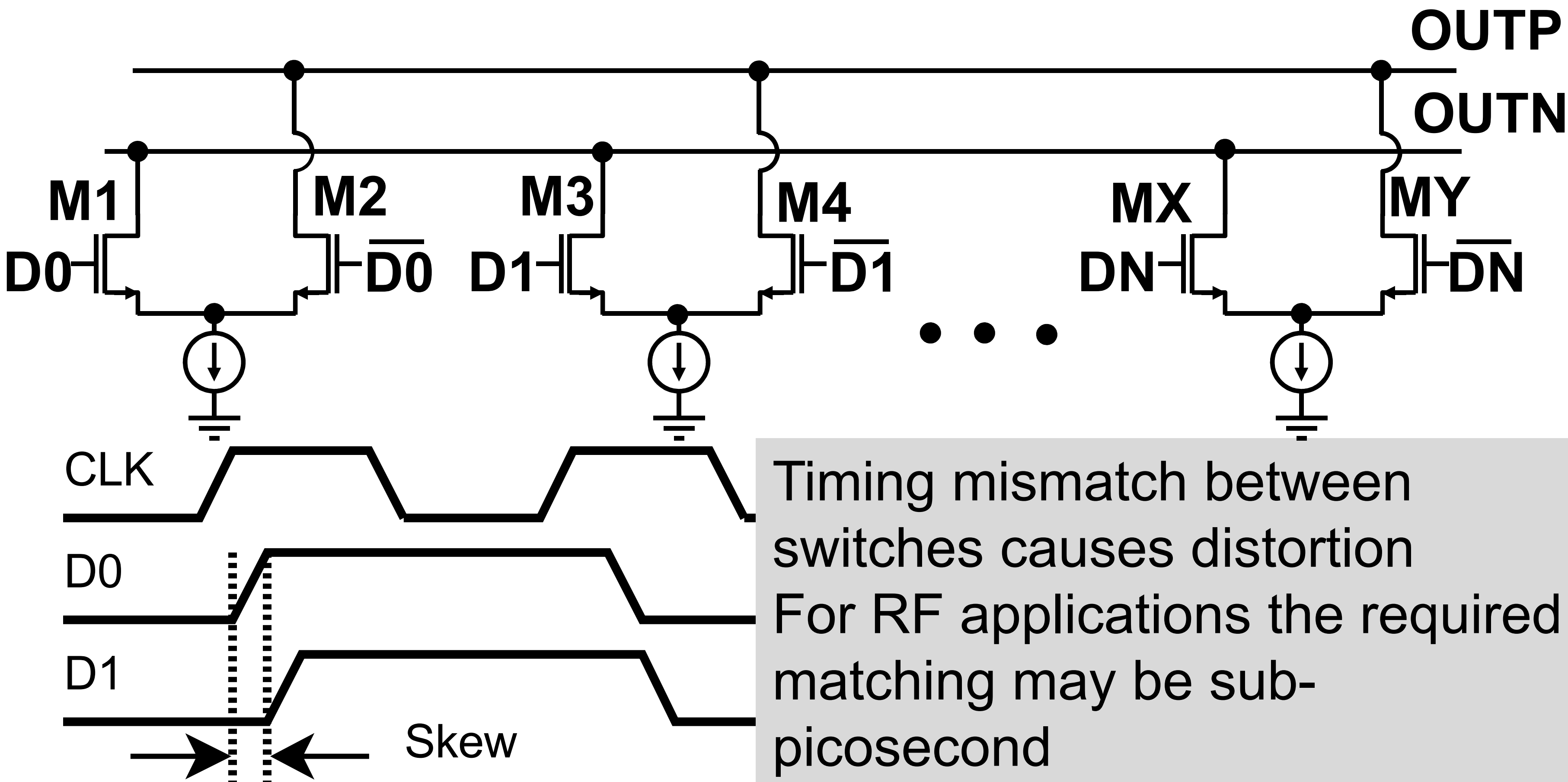
DUC+DAC Architecture



Interleaved DAC Architecture

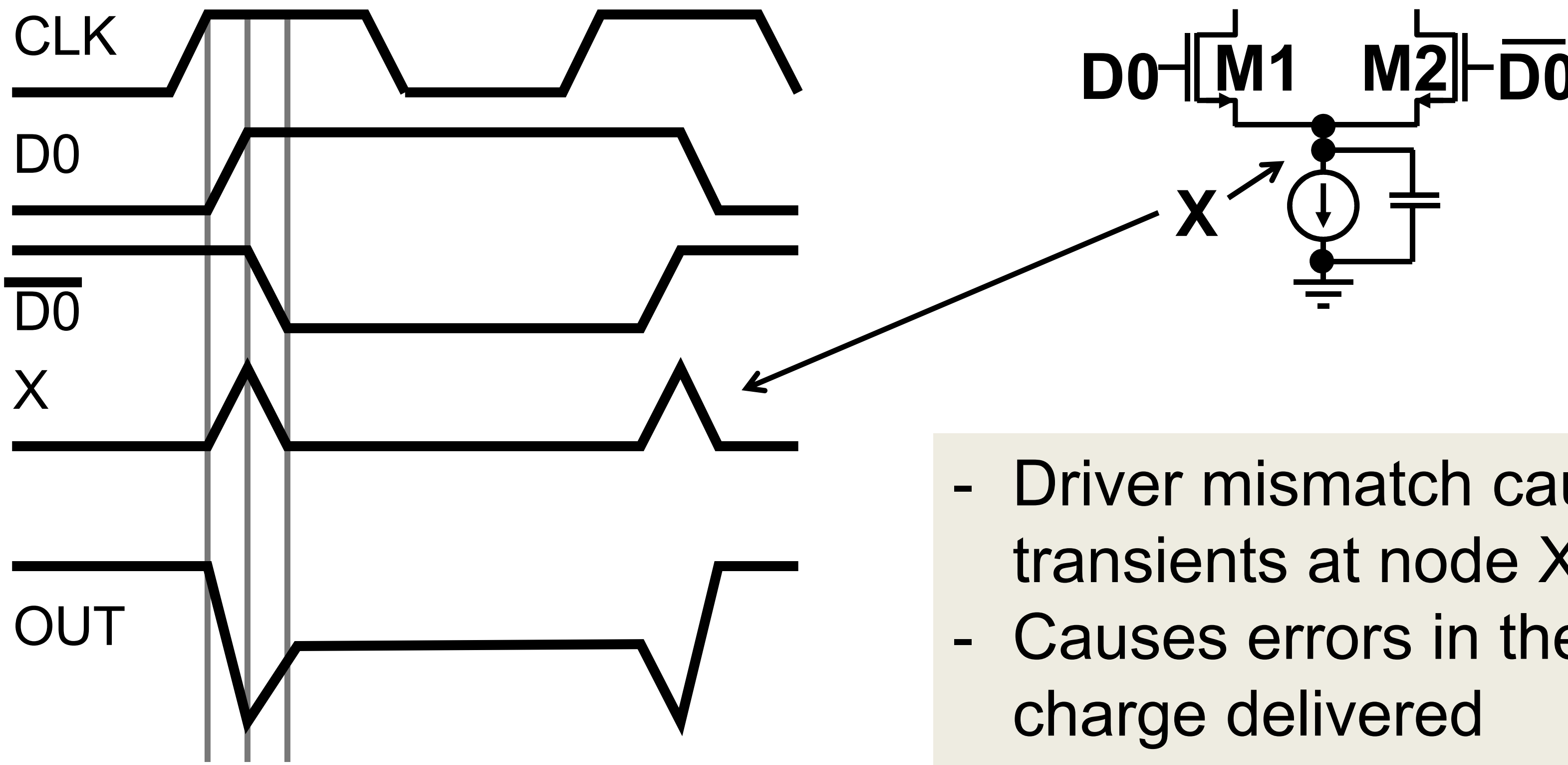
- Interleaving increases sample rate
- Attenuates timing skew induced distortion
- Attenuates other DAC transition related distortion

Timing Related Distortion in Current Steering DACs



- Timing mismatch between switches causes distortion
- For RF applications the required matching may be sub-picosecond

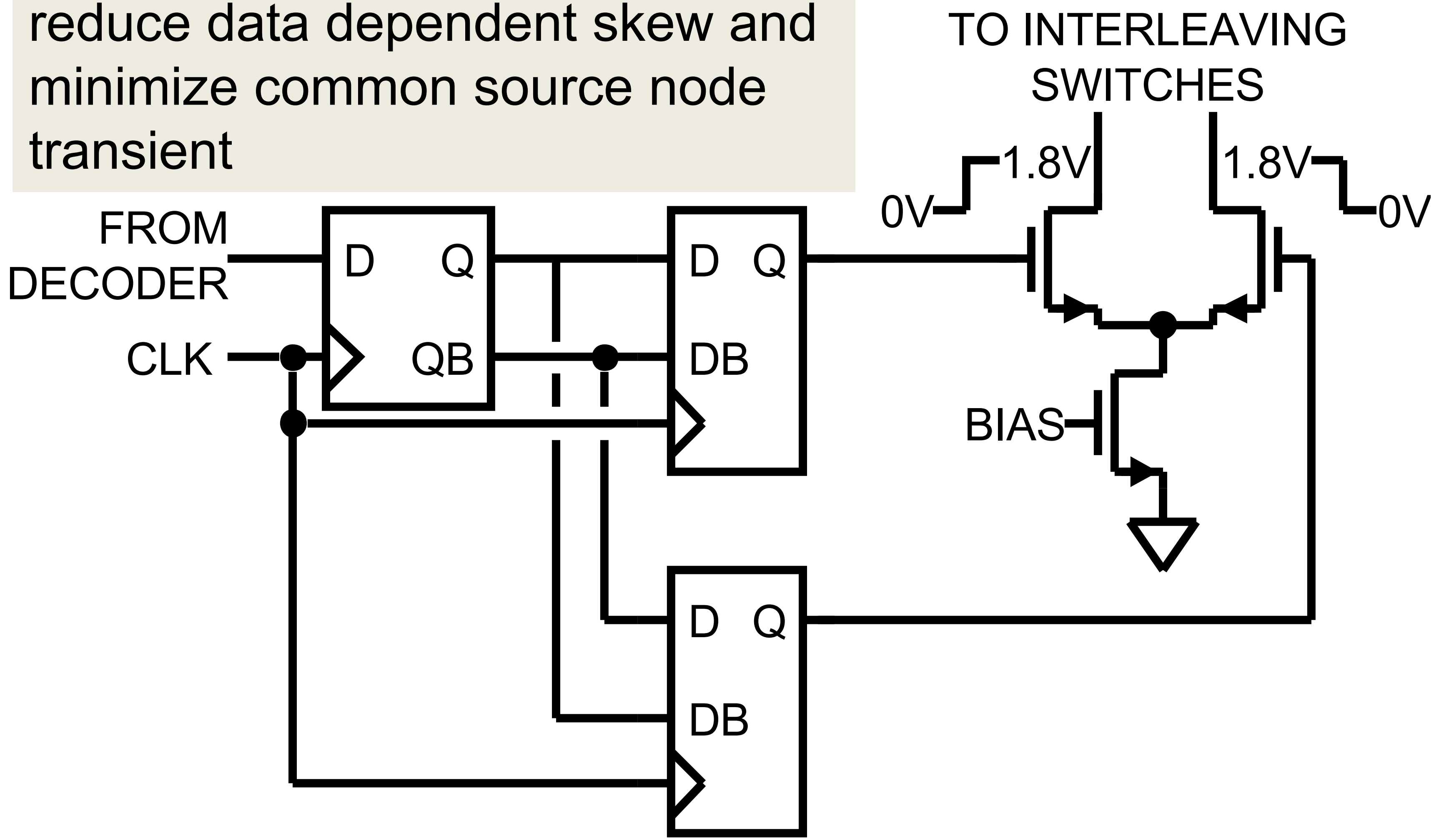
Transition Related Distortion in Current Steering DACs



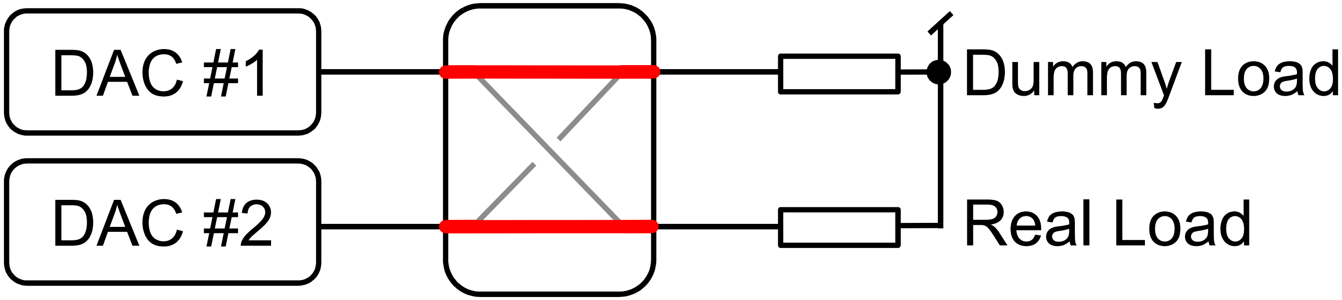
- Driver mismatch causes transients at node X
- Causes errors in the total charge delivered
- Worse as sample rate increases

Current Steering Switch Cell

Two stages of local retiming help reduce data dependent skew and minimize common source node transient

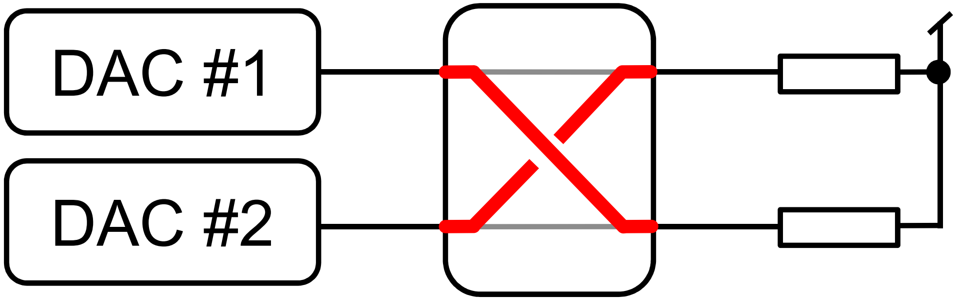


Analog Retiming and DAC Interleaving



- Solution: Interleave 2 DAC cores. Only connect a core to the final output after it has had ½ clock cycle to settle
- Benefits:
  - Attenuates timing skew between unit cells (switching occurs while DAC is connected to dummy load)
  - Attenuates transition related errors
  - Doubles the DAC update rate

Analog Retiming and DAC Interleaving



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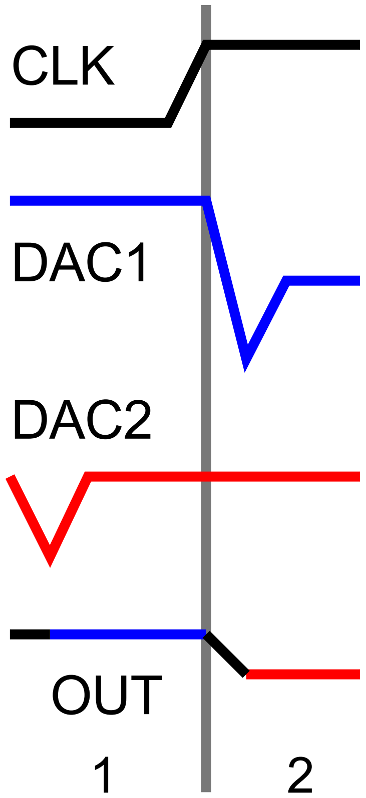
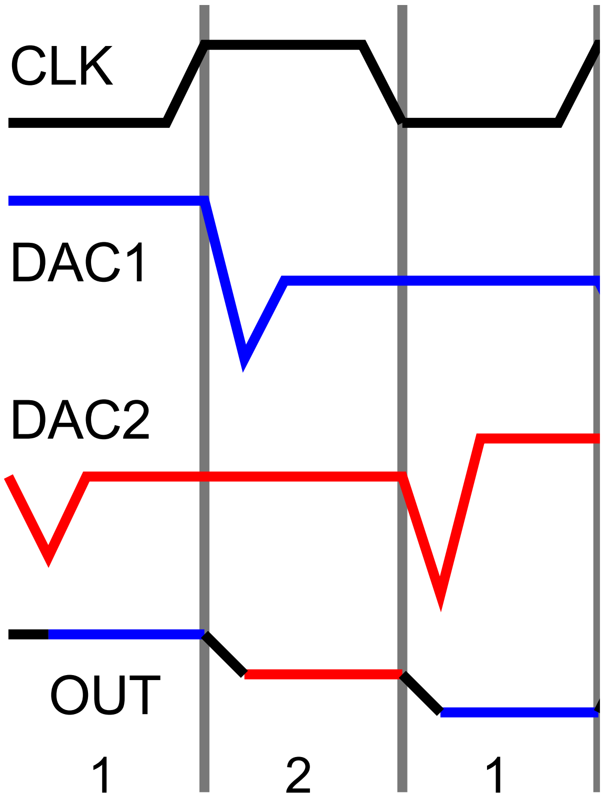


Analog Retiming and DAC Interleaving



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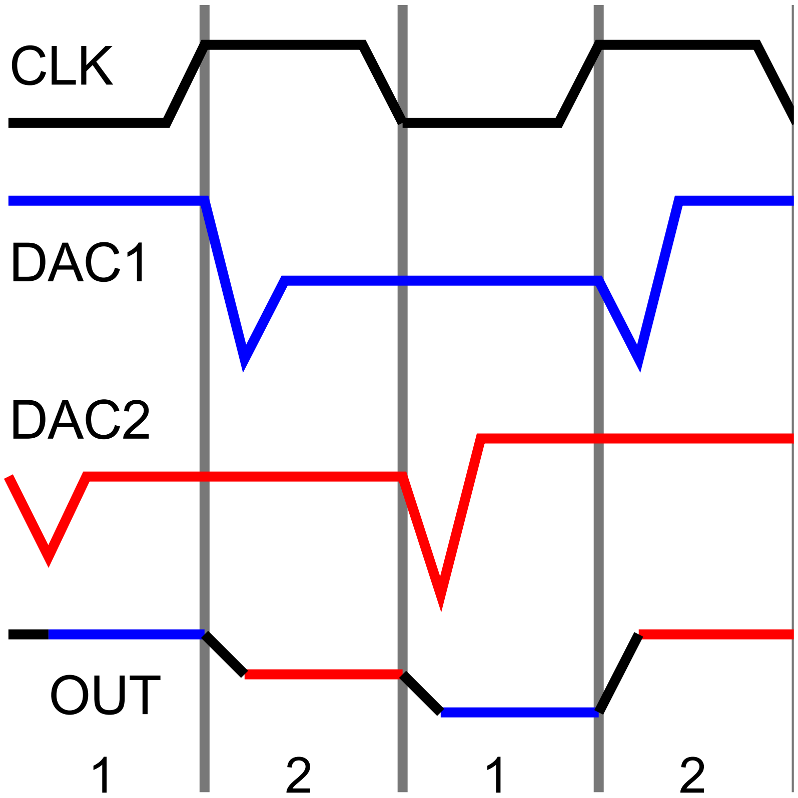
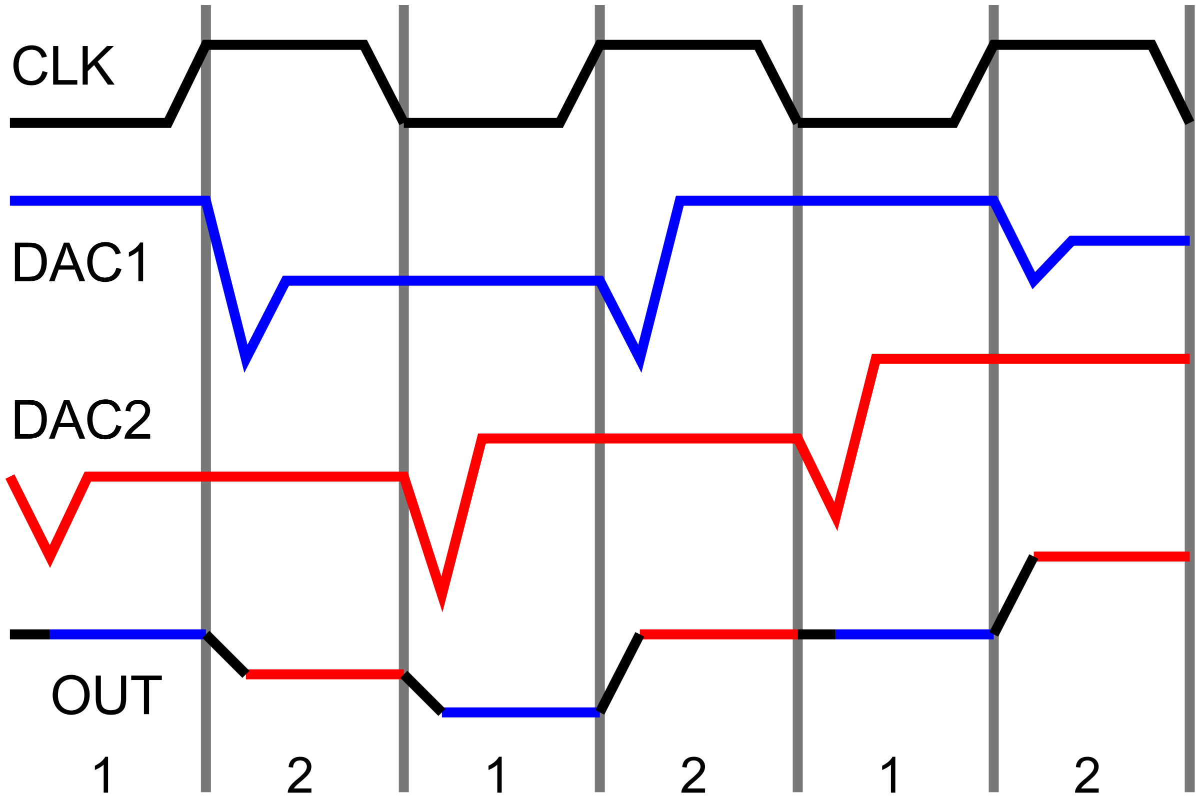
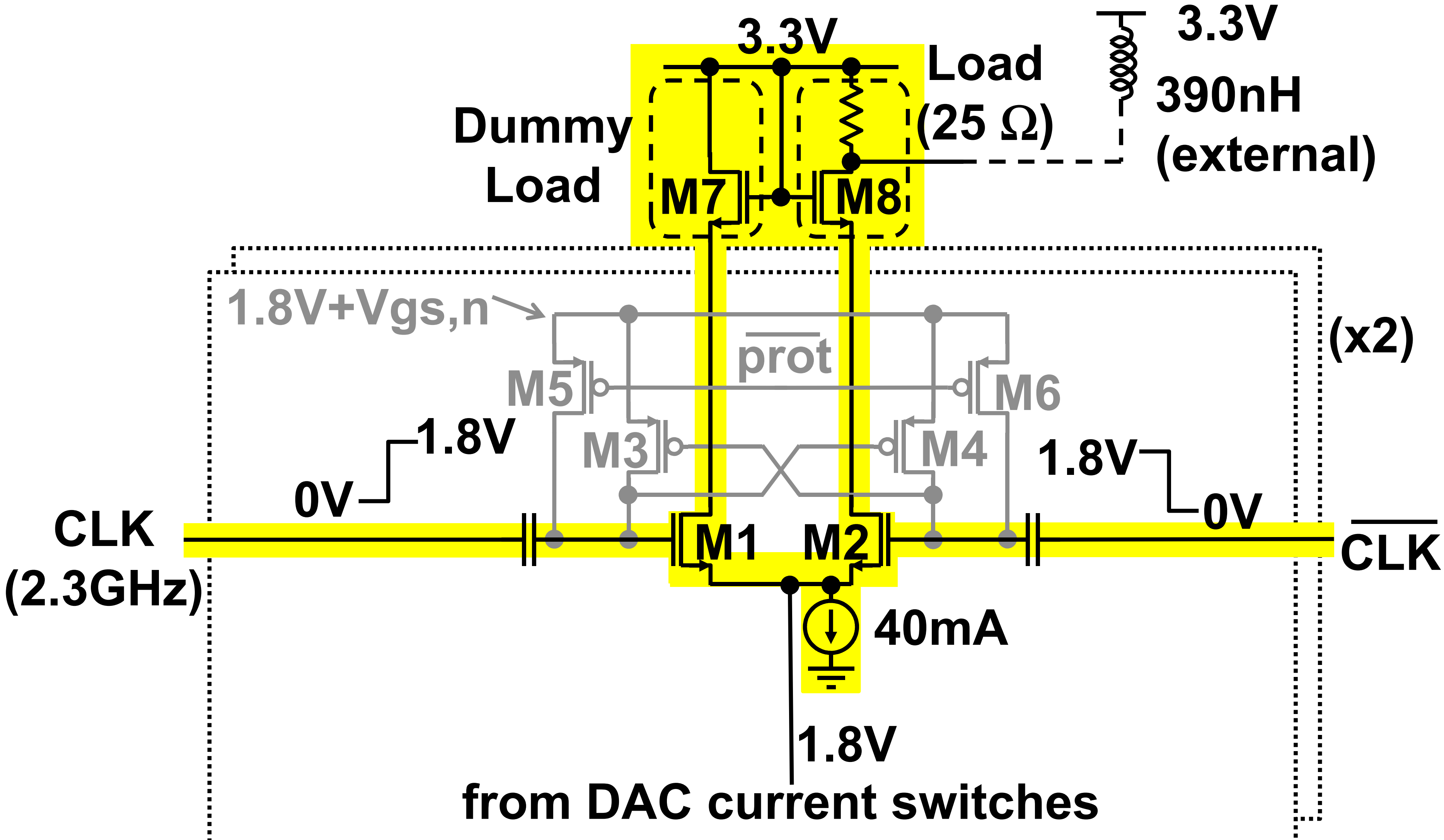


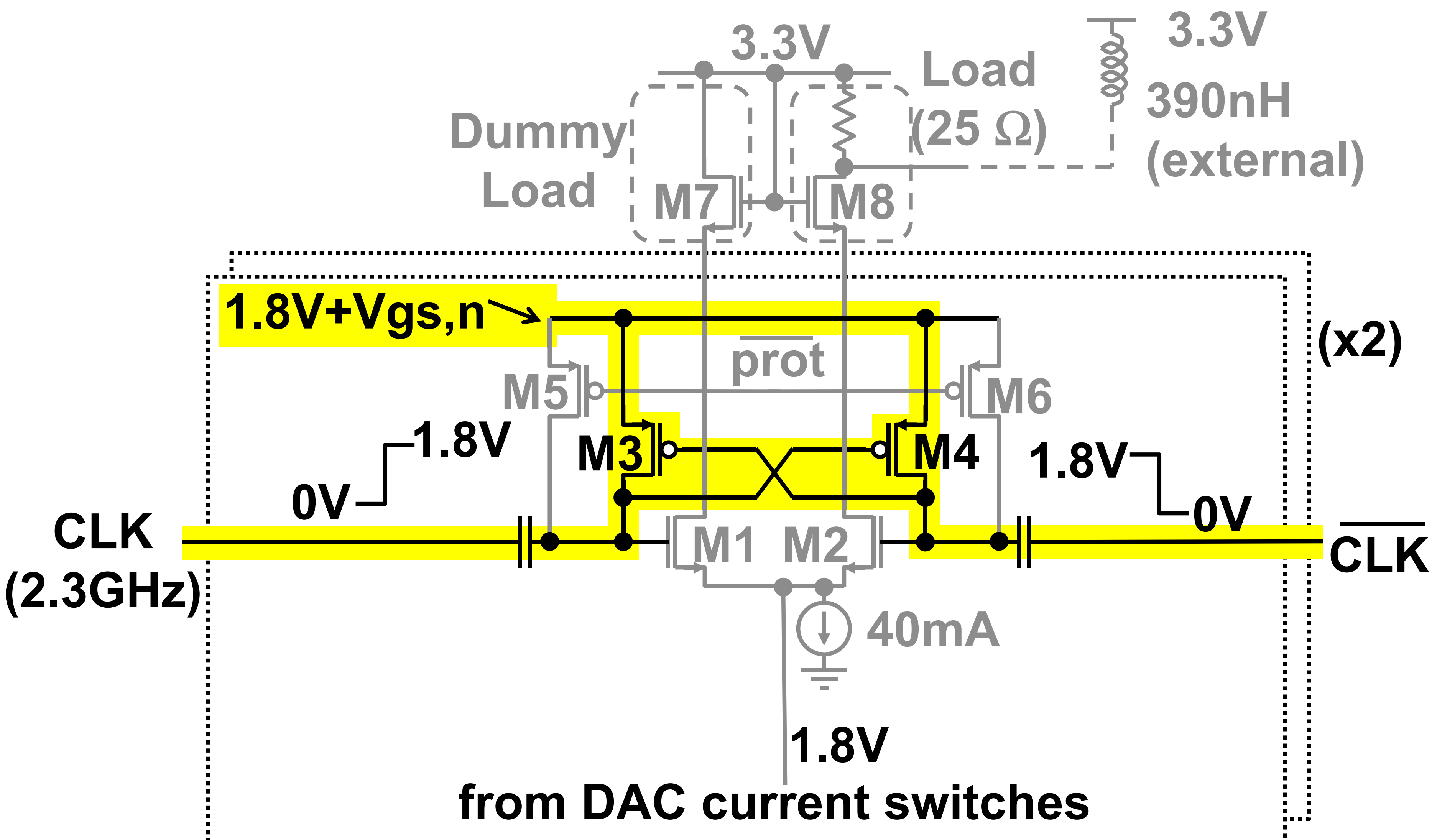
Analog Retiming and DAC Interleaving



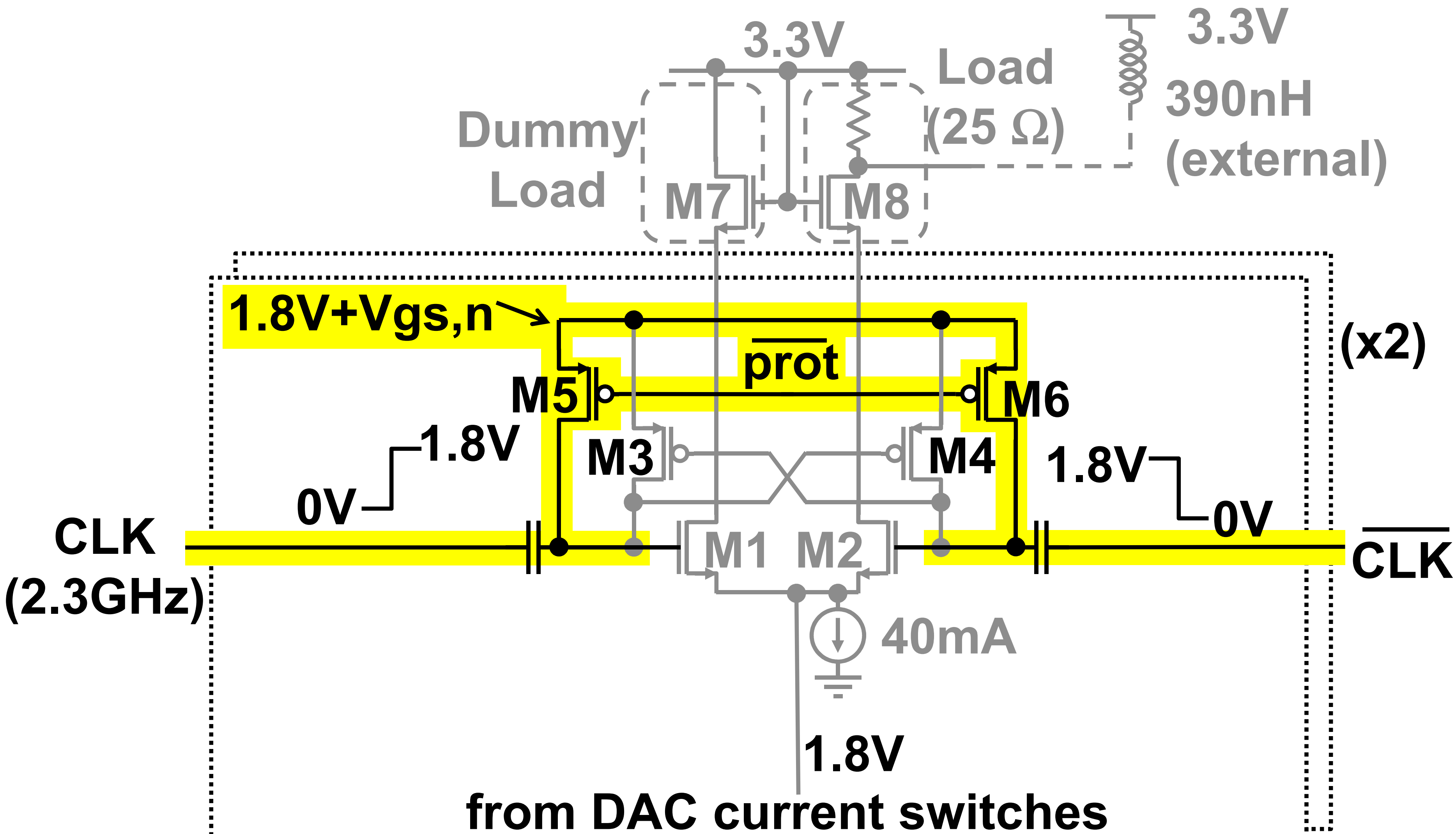
Interleaving Switch 1/2 Circuit



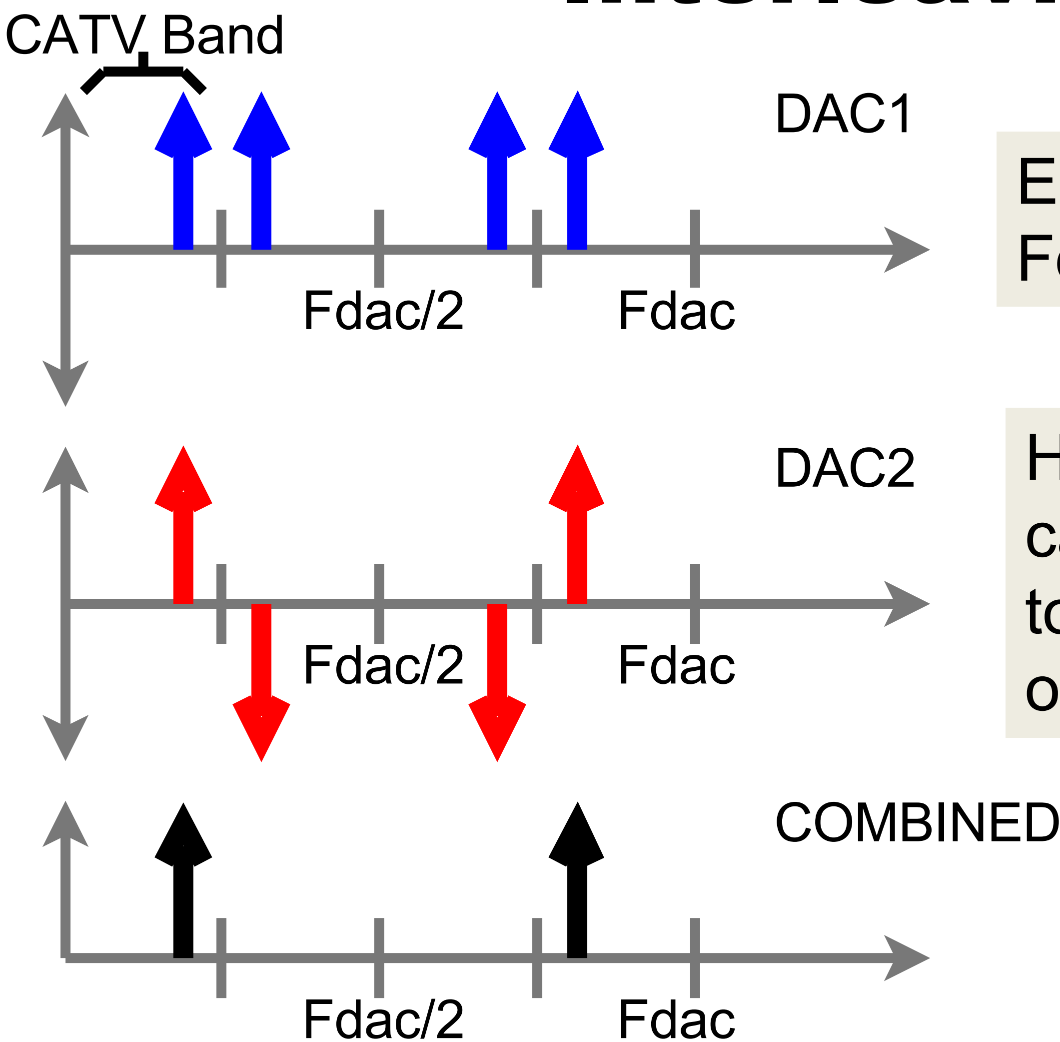
Interleaving Switch 1/2 Circuit



Interleaving Switch 1/2 Circuit



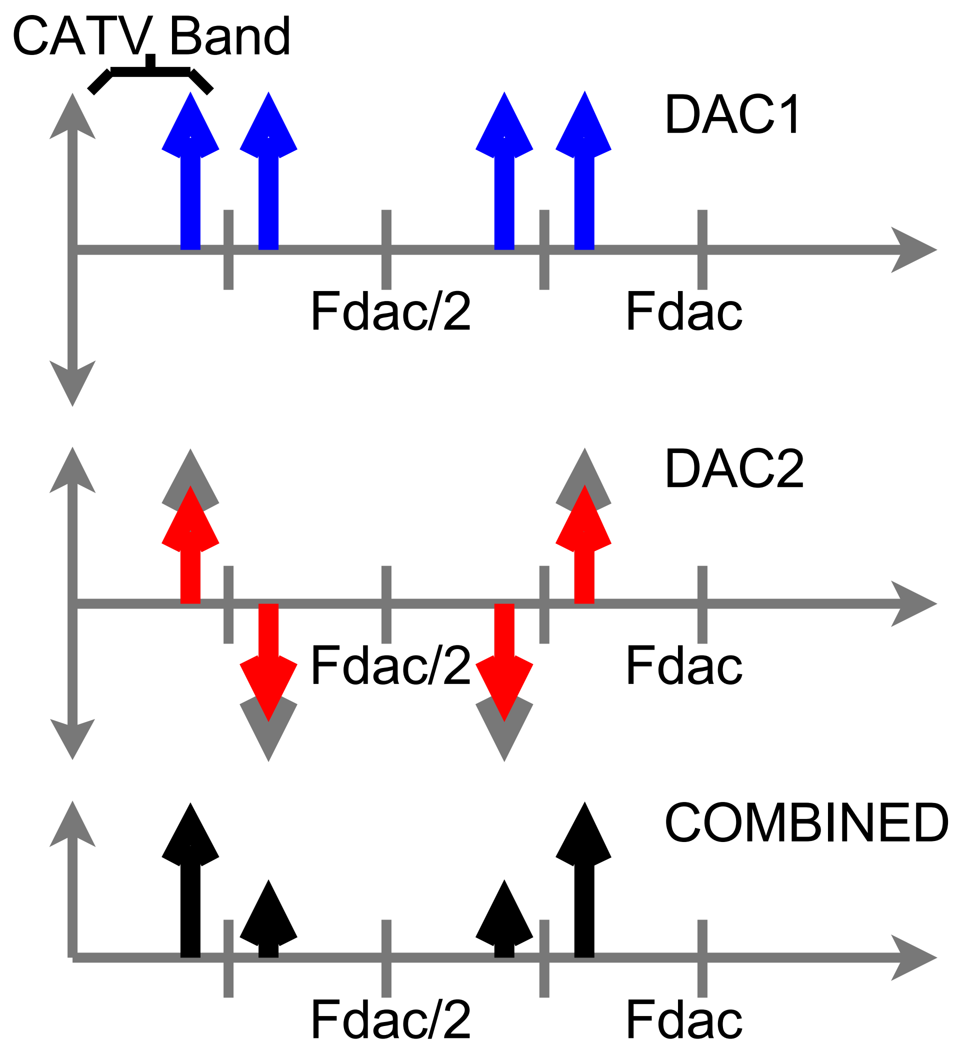
Spectral Viewpoint of Interleaving



Each DAC operates at Fdac/2

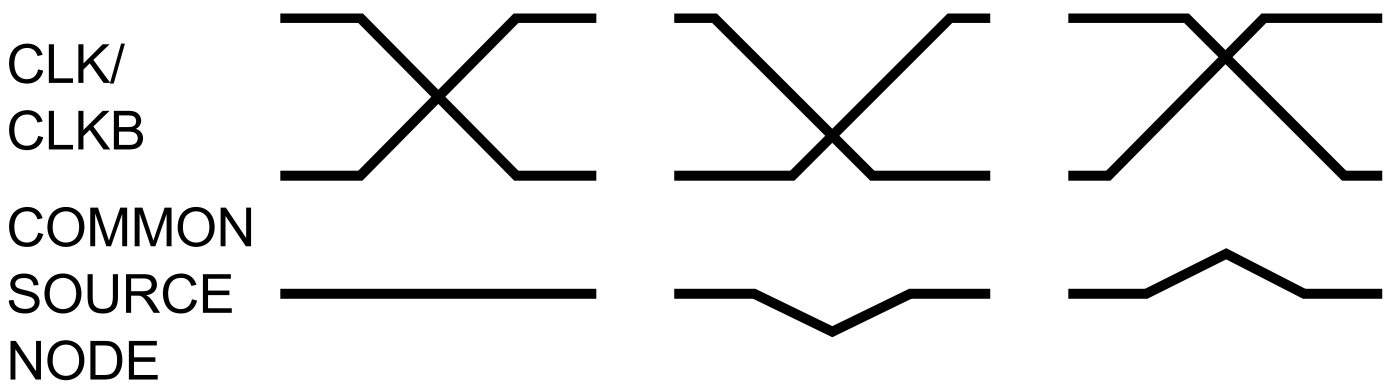
Half clock cycle delay causes DAC2 images to be 180 degrees out of phase from DAC1

DAC1/DAC2 Matching Effects

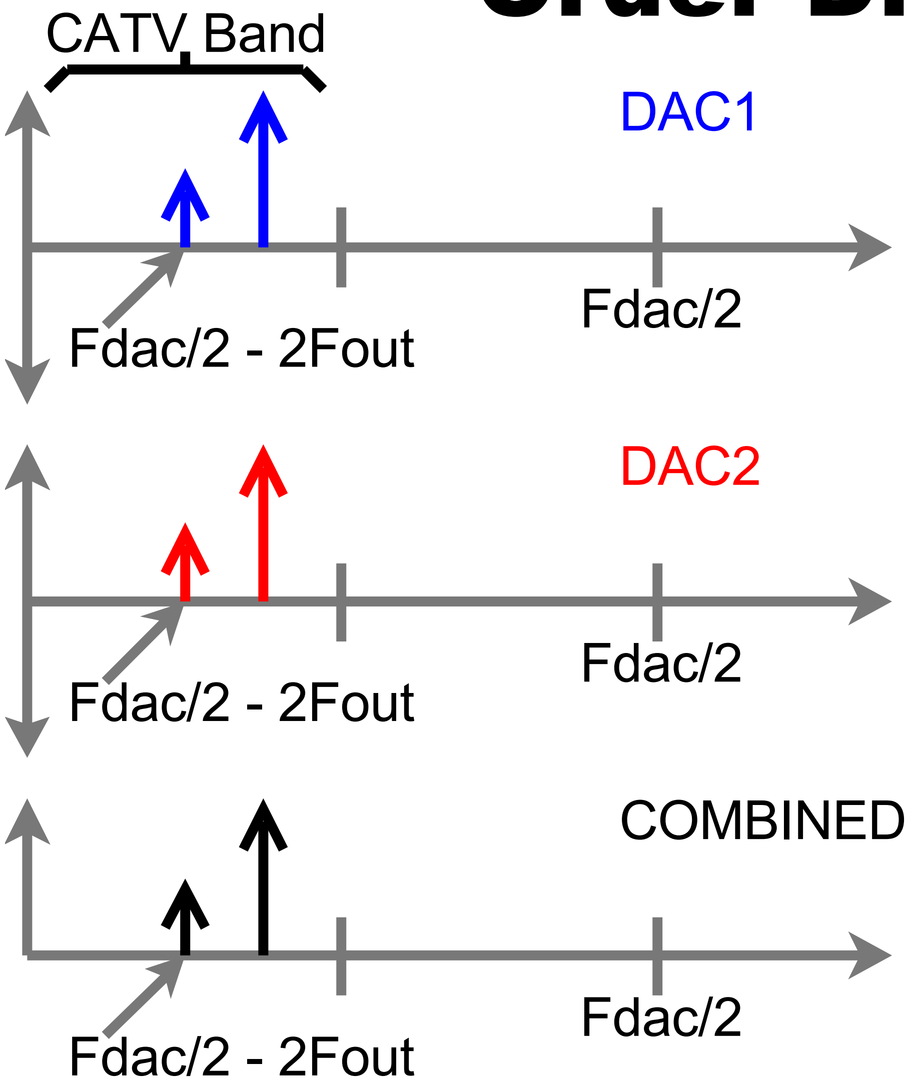


Interleaving Switch Cross Point

- The crossing point of the complementary clocks affects the common source transient in the interleaving switches
- Design for appropriate cross point



Interleaving Effects – Even Order Distortion



For Fout>650 MHz, Fdac/2-2*Fout is in band

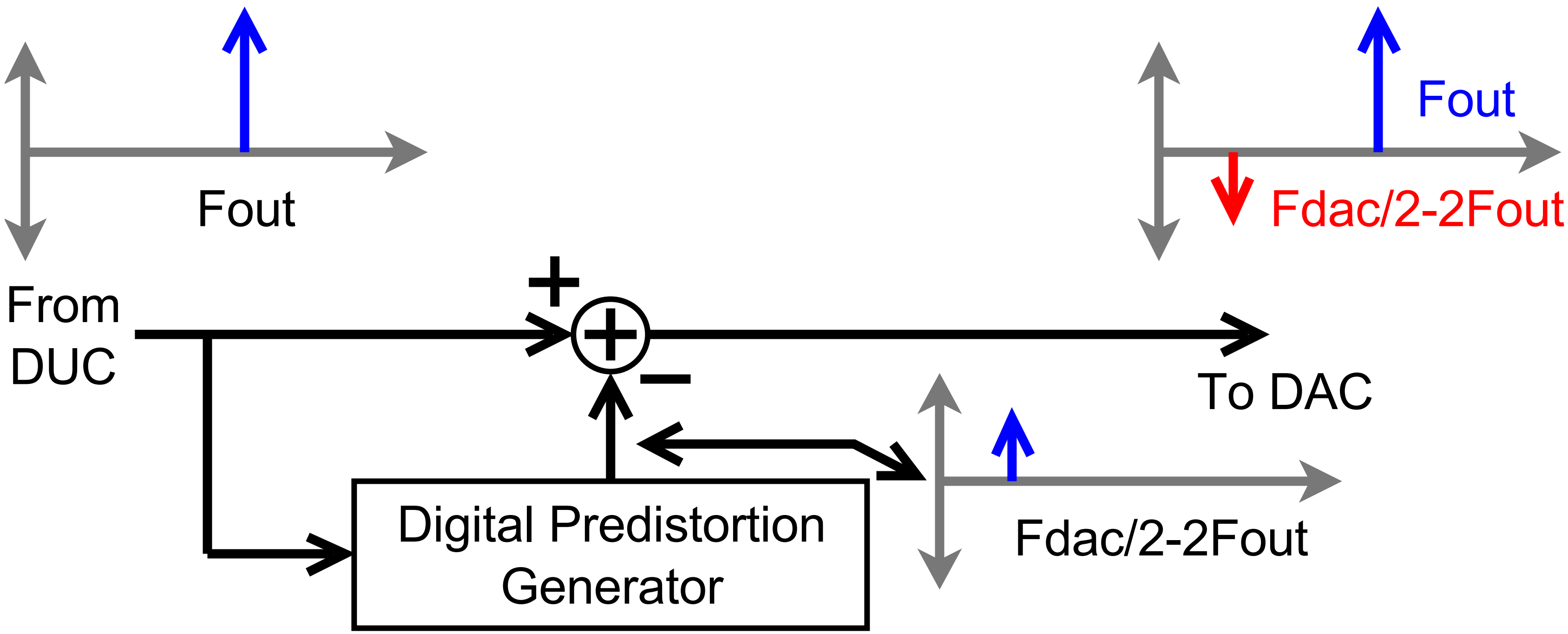
HD2 phase depends on the direction of +/- mismatch in the differential circuit

The HD2 phase of DAC2 may or may not be the opposite of DAC1

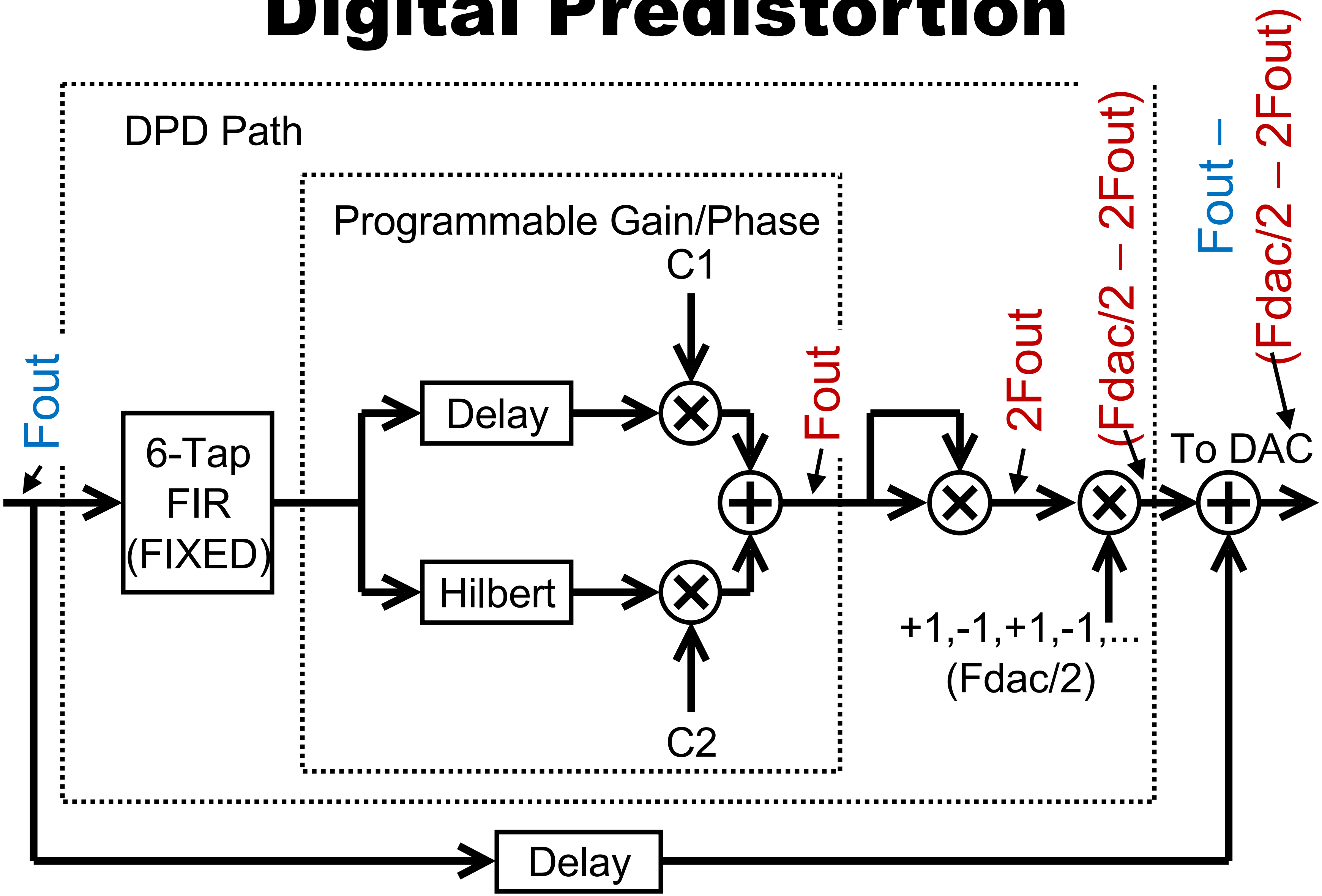
In general, we can't count on suppression of this spur by interleaving

Digital Predistortion (DPD)

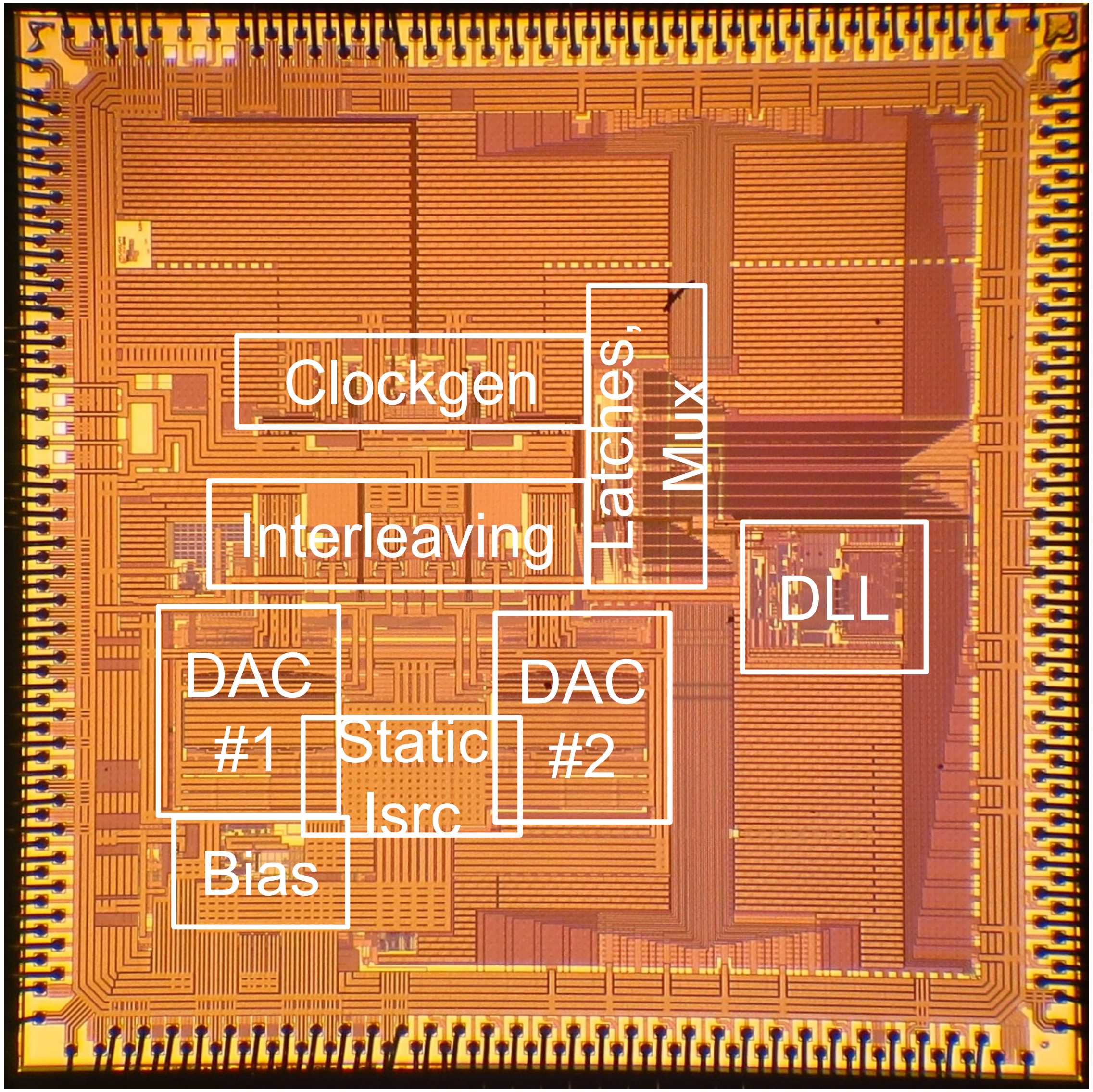
- DPD performed in 40nm where it is inexpensive
- Adds a small correction signal to the data before sending to the DAC



Digital Predistortion



Die Photo

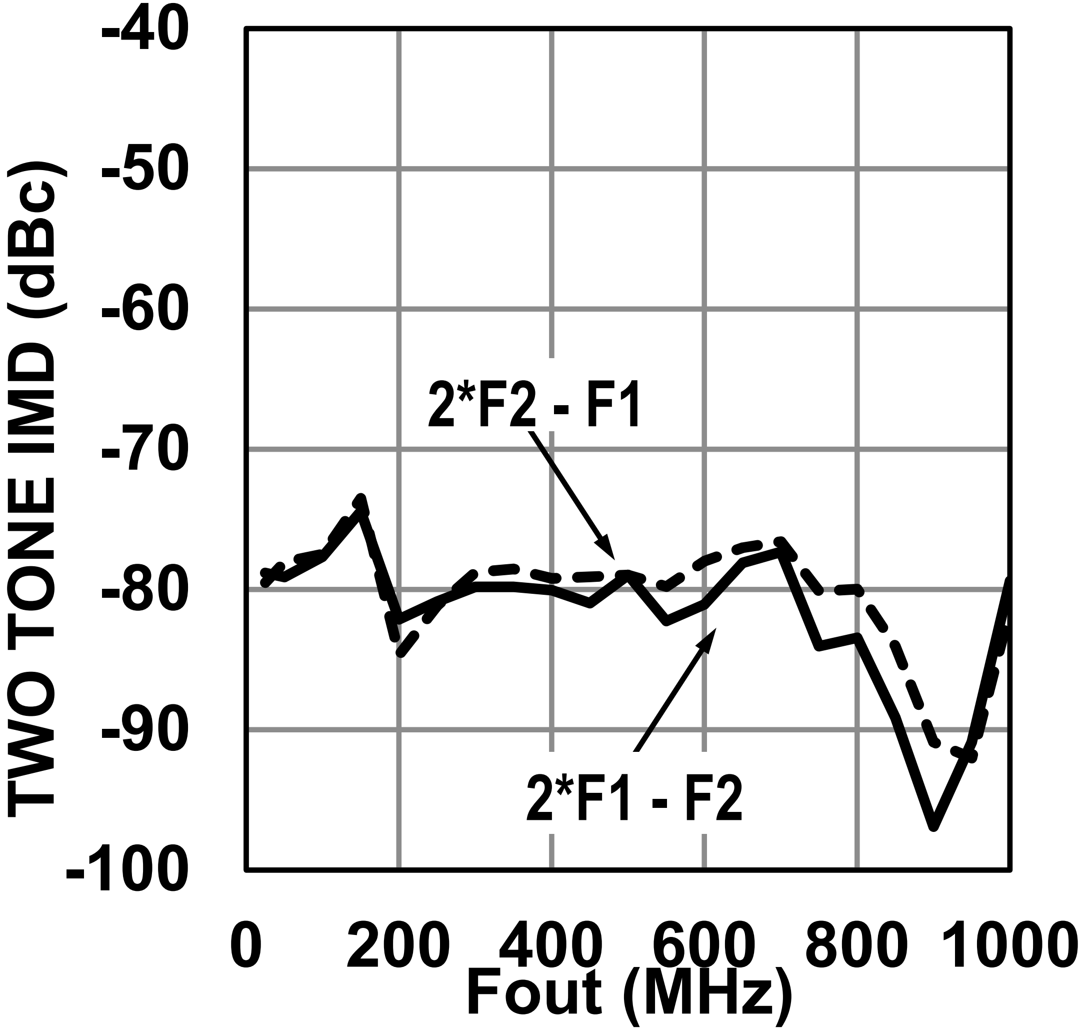


180 nm CMOS

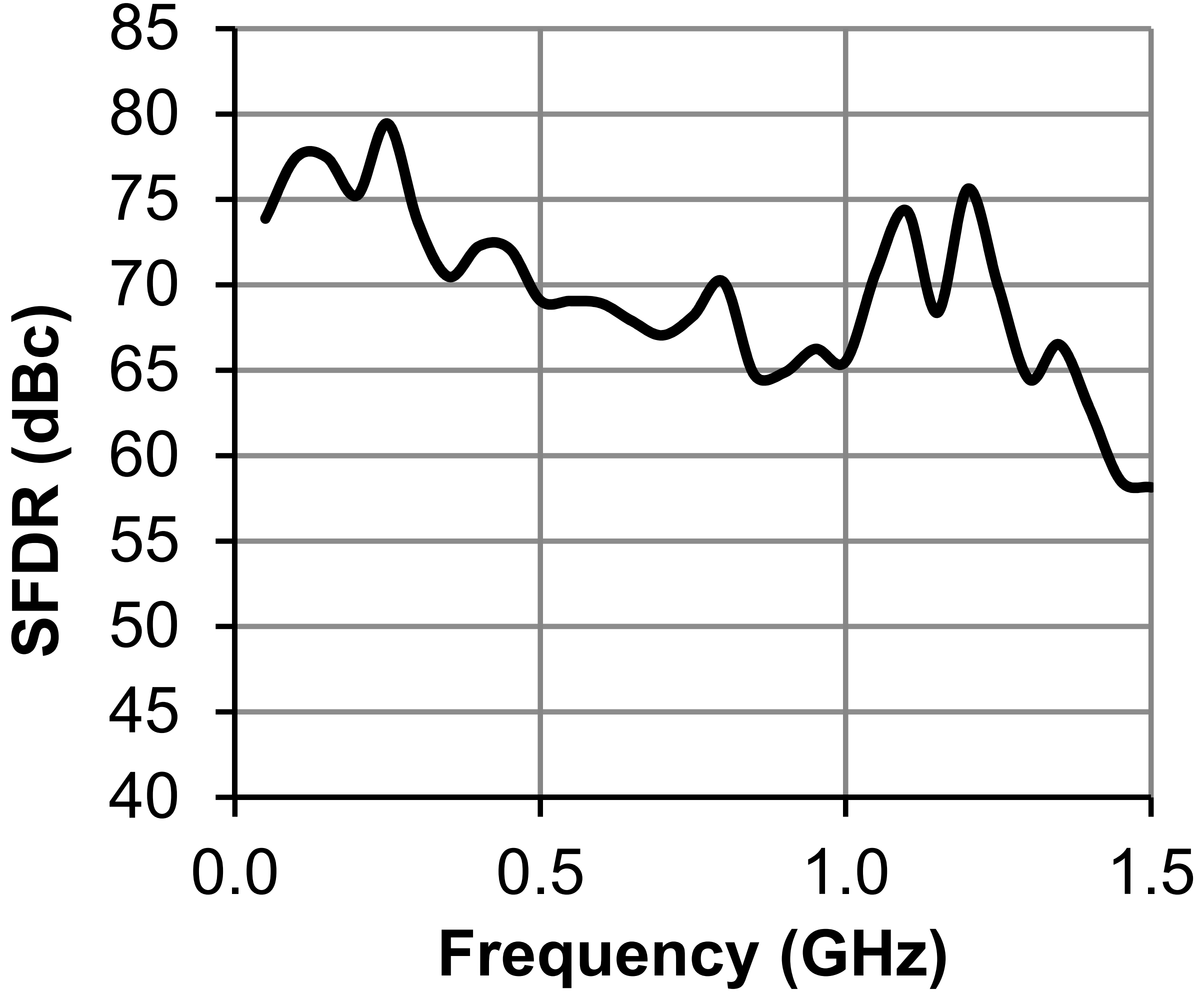
5.2 mm^2 active area.

Pad limited

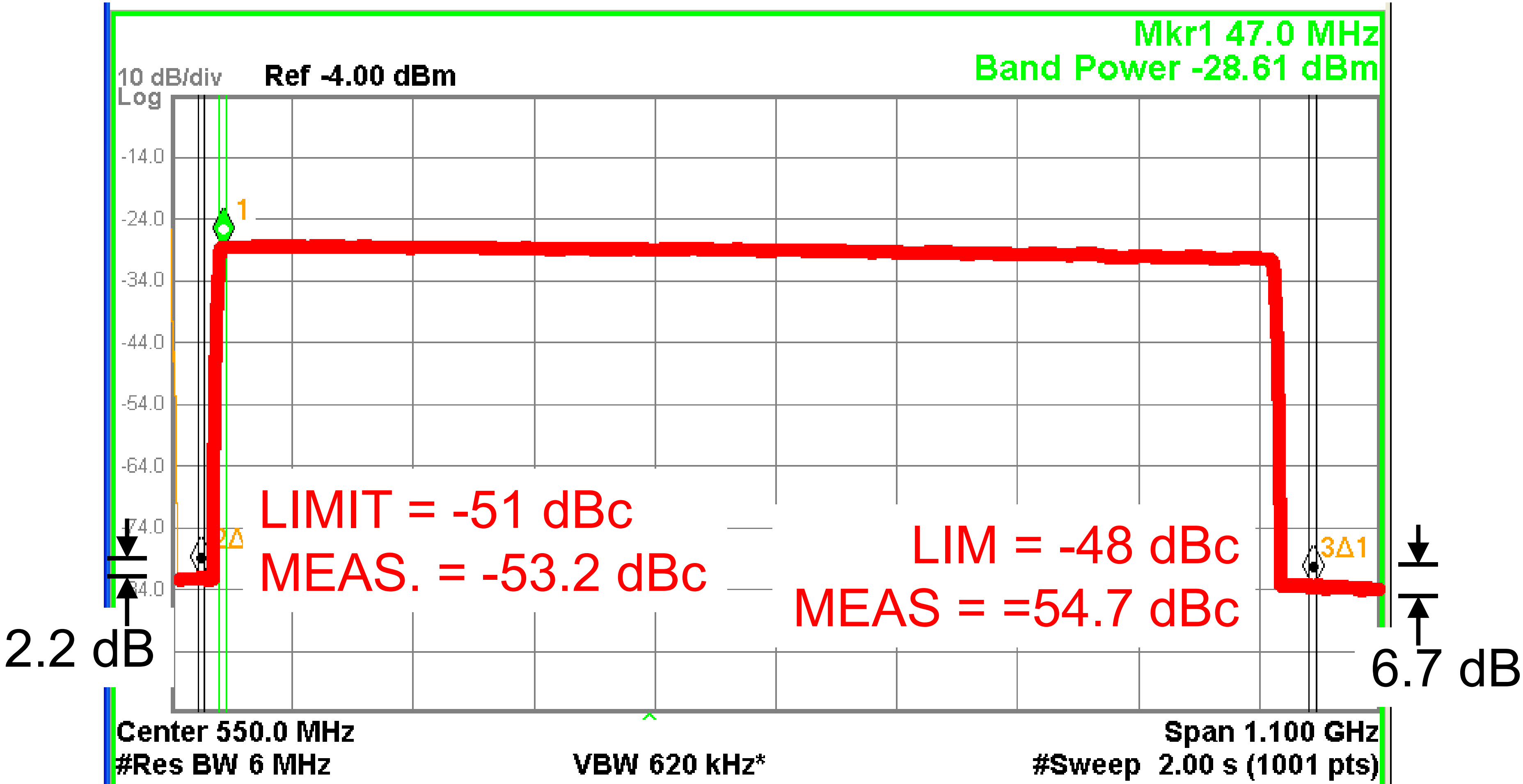
Experimental Results
2-Tone IMD



Experimental Results
SFDR

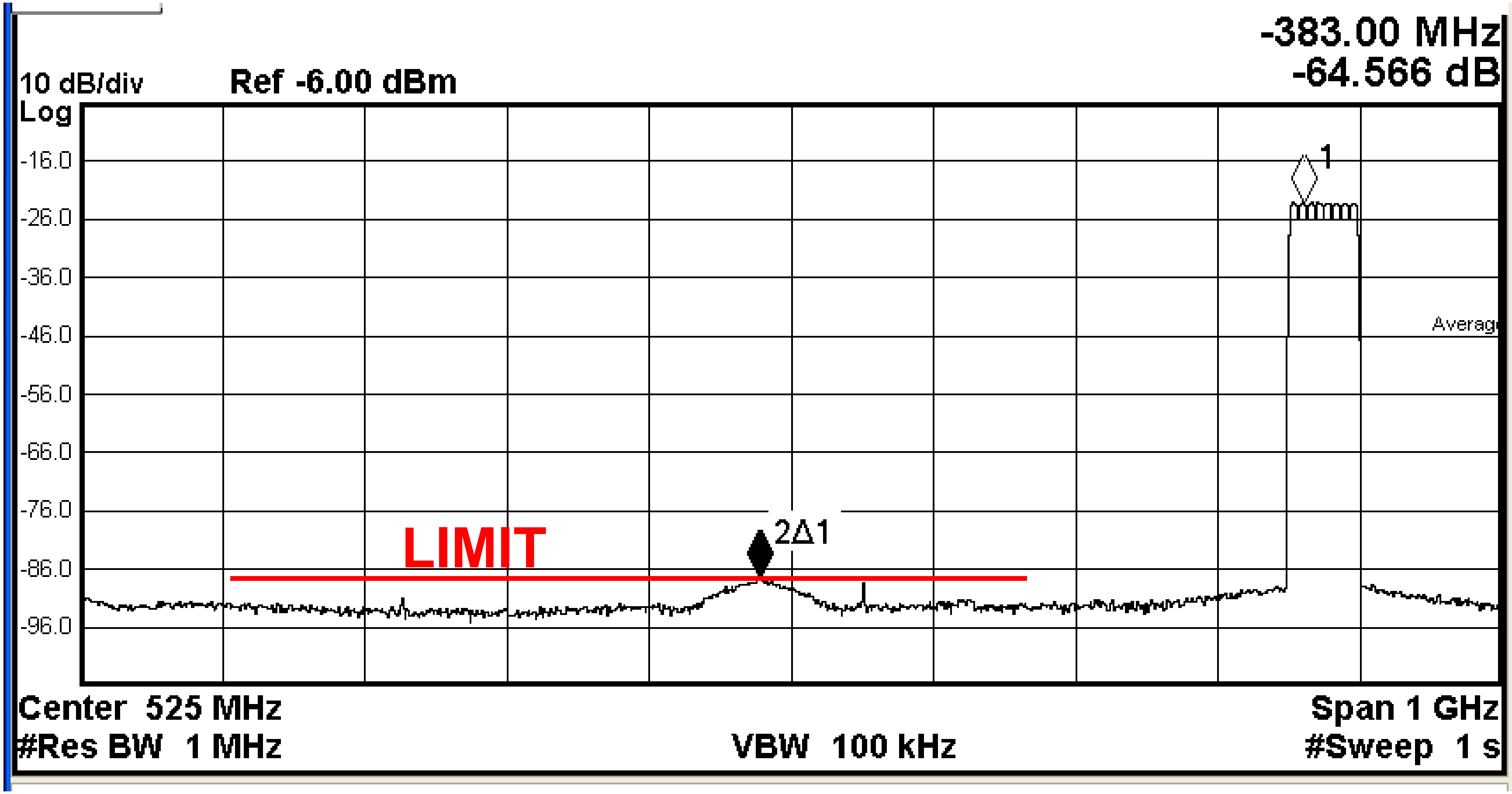


160 Channel QAM Results



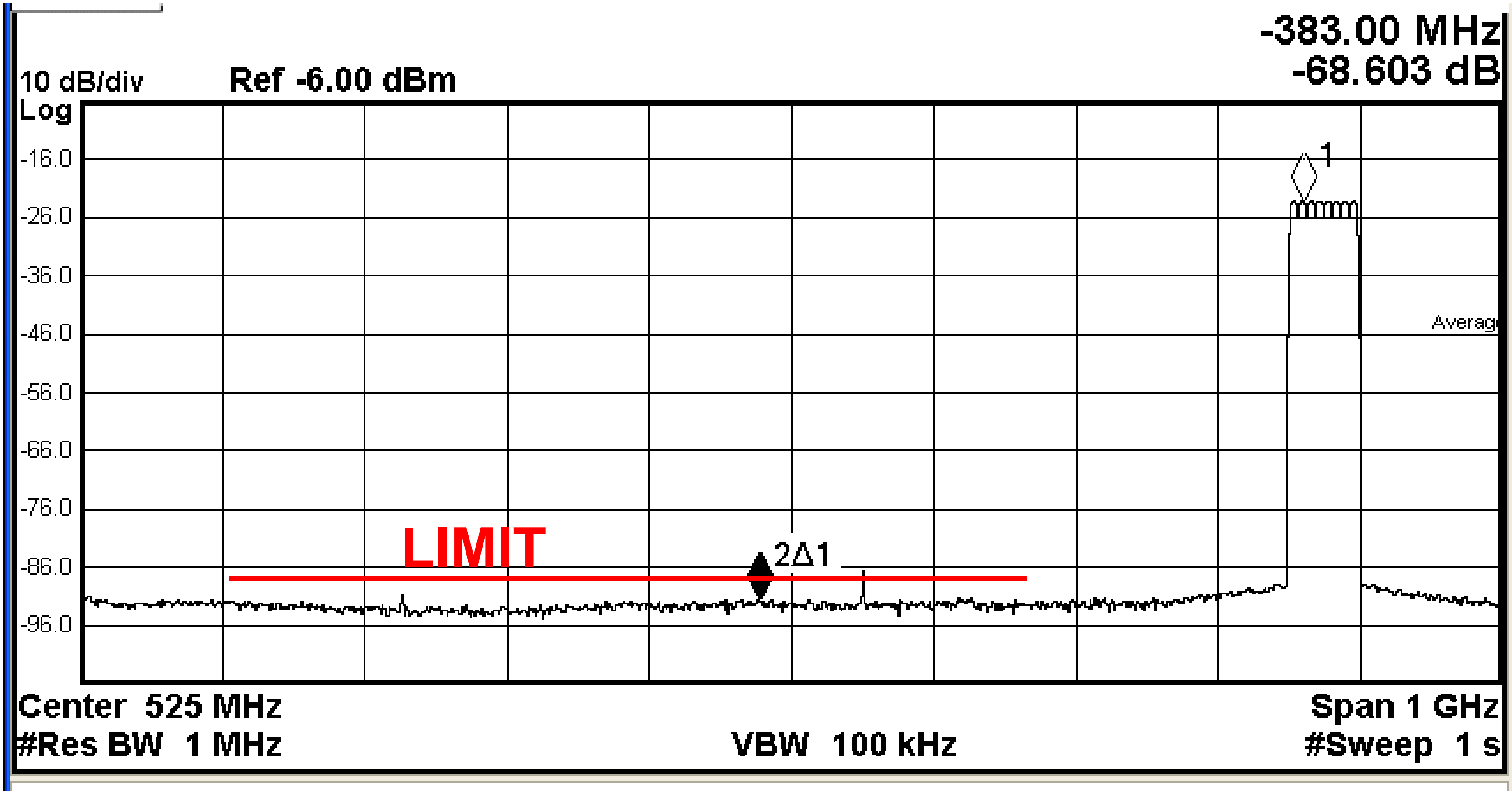
MKR	MODE	TRC	SCL		X		Y	FUNCTION	FUNCTION WIDTH		FUNCTION VALUE
1	N	1	f		47 MHz		-28.61 dBm	Band Power	6.000 MHz		-28.61 dBm
2	Δ1	1	f	(Δ)	-20.0 MHz	(Δ)	-53.18 dB	Band Power	6.000 MHz	(Δ)	-53.18 d
3	Δ1	1	f	(Δ)	991.4 MHz	(Δ)	-54.65 dB	Band Power	6.000 MHz	(Δ)	-54.65 d

Fdac/2-2*Fout – DPD OFF



4.6 Gsps, 900 MHz, 8 QAM Channels

Fdac/2-2*Fout – DPD ON



4.6 Gsps, 900 MHz, 8 QAM Channels

Measured Results

Parameter	This Work	[3]	[4]	[5]	[6]
Technology (nm)	180	180	90	65	40
Update Rate (GSPS)	4.6	3	1.25	2.9	1.6
Resolution (bits)	14	14	12	12	12
SFDR@500MHz (dBc)	69	60	70	52.5	73
IMD @500MHz (dBc)	-79	<-70		-72.5	<-70
DOCSIS ACPR (dBc)	55 (160 carriers)	52 (150 carriers)			
Output current (mA)	80	20	16	50	16
Power (mW)	2300	600	128	188	40
Vdd (V)	1.8, 3.3	1.8, –1.5	1.2, 2.5	1.0, 2.5	1.2
active area (mm^2)	5.2	4.0	0.83	0.31	0.016

Summary

- Demonstrated a complete DOCSIS compliant DUC+DAC combination
- High output power eliminates 1 stage of post amplification
- RF DAC implemented in a mature, cost effective technology
- Performance proven in production silicon
- Interleaving improves sample rate and distortion
- DPD further improves in-band spurious performance
- Generation of up to 160 QAM channels in a single package

Acknowledgments

- Jagdish Agrawal
- Kevin Brown
- Dave Busby
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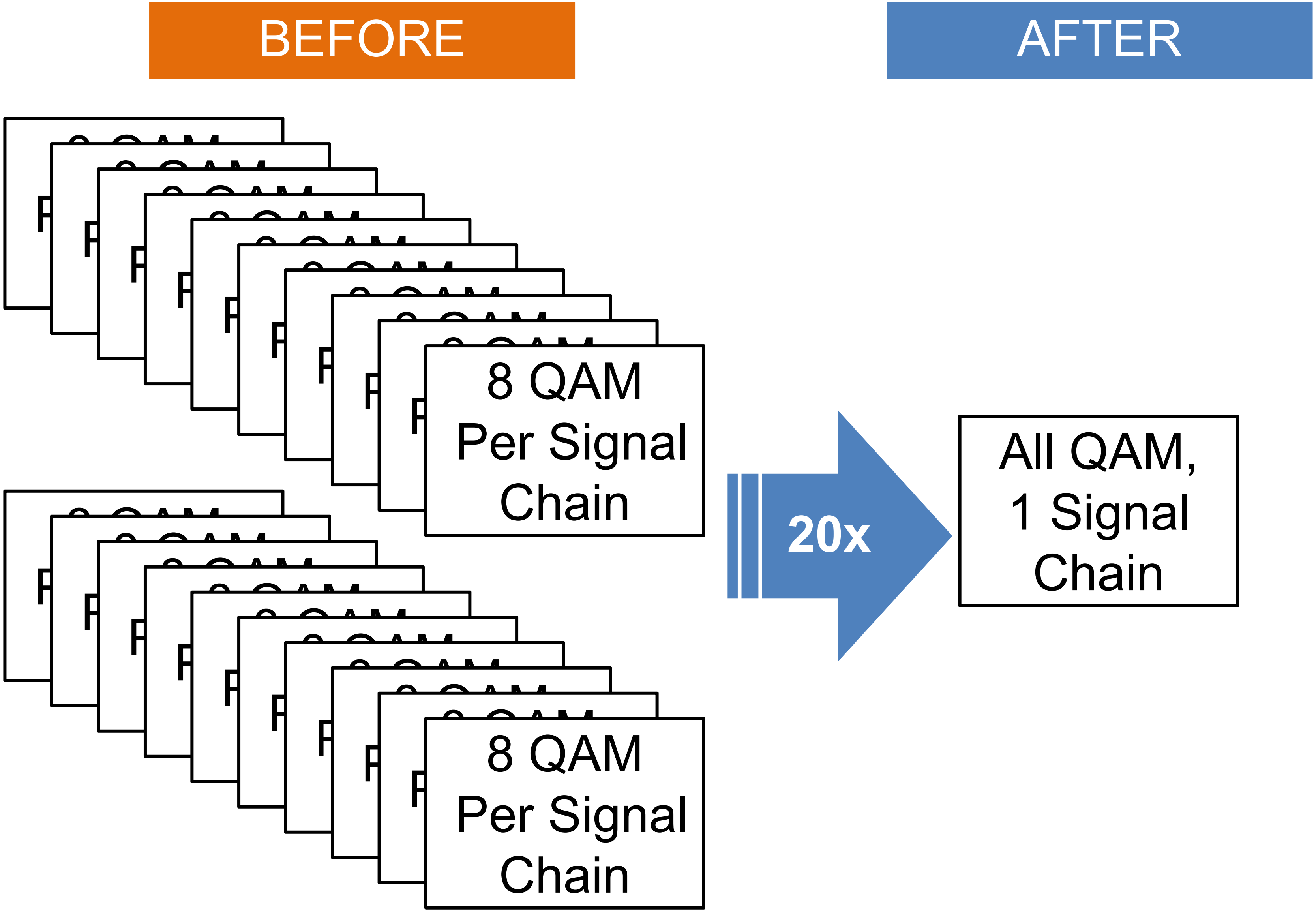
- Mike Cropp
- Jean Desrosiers
- Ed Gacek
- Shannon Horwitz
- Dwaine Hurta
- Paul Jones
- Prasanna Kunjar
- Joe Lutsky
- Suman Musunuru
- David Nielsen
- Jerzy Teterwak
- Scott Unger

Questions?



BEFORE
AFTER
8 QAM
Per Signal
Chain
8 QAM
Per Signal
Chain
20x
All QAM,
1 Signal
Chain